

© 2015 IEEE. REPRINTED, WITH PERMISSION, FROM

# **Next Generation Copper Pattern Plating for IC Package Application**

Makoto Sakai, Mutsuko Tamura, Toshiyuki Morinaga, Shinjiro Hayashi

Dow Electronic Materials

300 Onnado Agano City Niigata 959-1914 Japan

IMPACT Conference Proceedings, October 2015.

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Dow Electronic Materials' products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

# **ABSTRACT**

This paper describes the study of a new pattern plate, direct current (DC) electrolytic copper plating chemistry for IC package (PKG) application. The new chemistry shows good via-filling performance and good pattern plate uniformity together with thinner surface copper deposit. Also it shows excellent thermal reliability and good deposit physical properties. The new chemistry delivers high quality and high reliability for pattern plate for IC package application.

# INTRODUCTION

Miniaturization continues to be a defining trend in microelectronics. It is particularly prominent in the field of mobile devices. Increasing demand of mobile device capability and network infrastructure forces continuous growth of the IC package material market. To produce increasingly fine pitch design and build-up technology, the semi-additive processes (SAP) has been used widely for IC package substrate [1-4].

Electrolytic copper micro via hole (MVH) fill plating is an enabling technology used in high density interconnection (HDI) and fine patterning for IC PKG substrate applications. Pattern via-fill technology with thinner and more uniform surface copper deposits is required. The new acid copper product has to meet key plating performance criteria including good via-fill and good thickness distribution with thinner surface copper deposits.

# Acid Copper Plating Process

A typical acid copper plating bath contains copper sulfate, sulfuric acid, chloride ions and properly balanced organic additive components.

- Copper sulfate is the initial source of copper ions.
- · Sulfuric acid contributes to the overall conductivity of plating bath
- Chloride ions work in conjunction with carrier agent to suppress deposition and help refine the deposit morphology.

Generally there are three type of organic additives used in acid copper plating baths.

- Brightener gives bright and smooth appearance. It also improves physical properties. In via-filling processes, it accelerates copper deposition inside the via hole.
- Carrier exerts a suppression effect on the copper deposition reaction in the presence of chloride ions over a wide copper deposition current region. It also functions as a wetting agent.
- Leveler is a kind of polarizer, and it is like a carrier. However, the
  mechanism of adsorption to suppress copper deposition is different
  from a carrier. Since leveler preferentially suppresses deposition on
  outermost copper surface, it aids the brightener to promote copper
  deposition inside the via hole.

The organic additives have a large role in enhancing plating performance in DC plating. Appropriate additive selection imparts higher plating performance such as excellent via-filling. In order to maintain plating performance, the additive package and inorganic components have been controlled in a well balanced plating bath [5-7].

# **EXPERIMENTAL**

Via-filling performance

Via-filling performance was evaluated by cross section analysis. The filling ratio was calculated B/A in percent as shown in Figure 1.

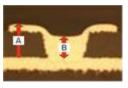


Figure 1 Measurement of via-filling performance

Deposition uniformity on pattern plate

The pattern design contains 10  $\mu m$  to 30  $\mu m$  width pattern lines, vias and pads. Deposition thicknesses on pattern lines, pads and land of vias were measured by a VK-8510 laser microscope (KEYENCE CO. Ltd.).



#### Physical properties

Approximately 50  $\mu m$  of deposit copper film was prepared, then annealed at 120 degrees C for 2 hours. The measurement of tensile strength and elongation were conducted using a 5564 Tensile strength meter (INSTRON Japan Co. Ltd. ).

# Thermal reliability

Solder float test tests were performed per IPC-TM650 2.6.8 as thermal shock resistance test to verify thermal reliability of plated vias on pattern boards. Solder shock conditions were 10 seconds float at 288 degrees C for 6 times. The samples were evaluated by cross section analysis after thermal shock.

# **RESULTS AND DISCUSSION**

#### Performance comparison on pattern plate

Via-filling performance

Figure 2 shows via-filling performance of two products. The new developed chemistry was able to fill vias with thinner surface copper deposition than the conventional product.

Via size	60 um diameter x 40 um depth		
X-section			
Surface thickness	9 µm	12 µm	
Filling ratio	90 %	90 %	
Current density	1.5 ASD		
Product	New product	Conventional Product	

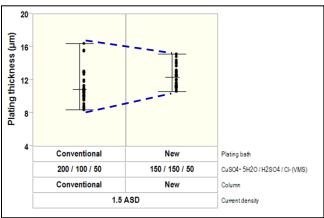
Figure 2 Via-filling cross section analysis of conventional product compared to the new product

Figure 3 and Figure 4 shows the pattern plating performance of our two chemistries with the same deposition thickness target.

Deposition thicknesses at various points were collected to evaluate plating thickness distribution in a piece of package.

New chemistry showed not only good via-filling ratio as well as conventional chemistry but also narrower deposition thickness range than conventional product.

Deposition uniformity on pattern plate



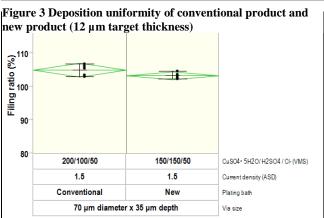


Figure 4 Via-filling performance of conventional chemistry and new chemistry (12  $\mu m$  target thickness)

Via-filling performance capability

Figure 5 and Figure 6 show the via-filling performance as a function of plating thickness for the two chemistries studied.

The bottom-up plating in the via hole was observed even after 4  $\mu$ m deposition thickness was obtained on the surface with the new chemistry. The via hole was almost filled with the deposited copper at the 6  $\mu$ m condition. The new chemistry showed complete via-filling at the 9  $\mu$ m condition.

New chemistry gave bottom-up deposition in via holes on thinner surface deposition phase. Consequently, it can deliver full filled via on thinner surface deposition than conventional product.

In terms of inorganic composition, new chemistry formulated with lower concentration of copper and higher acid in virgin make-up solution (VMS) compared with conventional chemistry. In general, higher concentration of copper and lower acid in VMS shows positive effect for via-filling performance. However, new chemistry showed faster via-filling compared with conventional product.

Also, new chemistry showed good bottom-up shape in via holes. It can mitigate voiding issue for reliable electrical connections. It was an important aspect of this via-fill technology. The results verified clearly that superior via-filling performance of new chemistry.



The results indicated new chemistry delivers high quality plating on pattern via-filling process.

Via size	60 um diameter x 40 um depth				
Plating thickness	2 μm	4 μm	6 µm	9 µm	12 µm
New		7			-
Conventional			3	~	~

Figure 5 Via-filling performance as a function of copper deposition thickness at 1.5 ASD

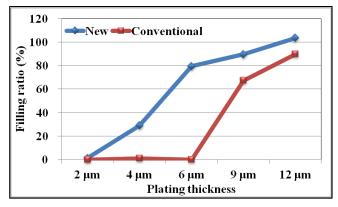


Figure 6 Filing ratio as a function of copper deposition thickness at  $1.5\ ASD$ 

Figure 7 and Figure 8 show via-filling performance as a function of current density of two our chemistries. New one showed good via-filling performance with thinner surface deposition than conventional product even at higher current density condition at 2 ASD.

The results indicated new product has potential to contribute high productivity.

Via size	60 um diameter x 40 um depth			
Current density	1.5 ASD		2.0 ASD	
Plating thickness	9 µm	12 µm	9 μm	12 µm
New				
Conventional	~	~	~	

Figure 7 Via-filling performance as a function of current density

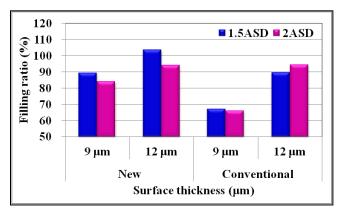


Figure 8 Filing ratio as function of copper deposition thickness and current density

#### Robustness of plating bath

Plating performance on pattern plate

The pattern panels were processed in a pilot plant scale plating cell at bath ages from 0 to 100~A-Hr/L.

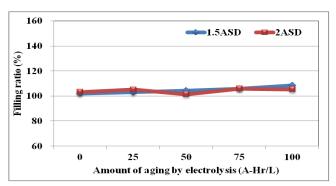


Figure 9 Via-filling performance as a function of aging

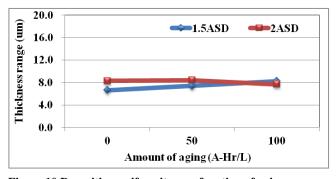


Figure 10 Deposition uniformity as a function of aging

As the results, satisfied and consistent via-filling performance was maintained by new chemistry during the bath aging. It also demonstrated consistent deposition uniformity in a piece of package during the bath aging.



#### Thermal reliability

The reliability of electroplated copper layer is an important quality criterion. No crack or any defect was observed on copper filled vias during bath aging as shown in Figure 11.

Via size	70 μm diameter x 35 μm depth		
Plating thickness	12μm target		
Amount of aging	0 A-Hr/L	50 A-Hr/L	100 A-Hr/L
1.5ASD	Passed	Passed	Passed
2 ASD	Passed	Passed	Passed

Figure 11 Solder float test results

#### Deposit physical properties

Tensile strength and elongation at each current density were consistent and satisfied value during bath aging. The results supported good reliability results of solder float tests.

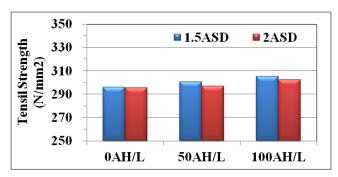


Figure 12 The results of tensile strength measurement

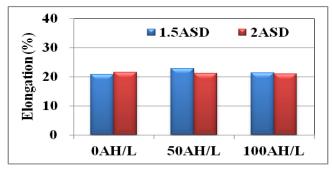


Figure 13 The results of elongation measurement

New product demonstrated consistent and good via-filling performance, deposition uniformity, thermal reliability and physical properties during aging. There was no failure on pattern plating performance during bath aging. The results verified good robustness of the plating bath with new chemistry.

#### CONCLUSION

This new product is designed for pattern via-fill application with thinner deposition. The main characteristics of this new chemistry are shown below.

- Excellent via-filling performance with thinner surface copper deposition
- > Faster bottom-up fill without void defect
- > Enhanced deposition uniformity
- > Excellent thermal reliability performance
- ➤ All additive components can be monitored by Cyclic Voltammetric Stripping (CVS) analysis

Since the newly developed chemistry is in an early stage of development it is also important to note the combination of specialized plating equipment and new chemistry optimization that enables various pattern designs or specifications on IC PKG application.

# **REFFERENCE**

- [1]M. Lefebvre, et al. "Copper Electroplating Technology for Microvia Filling", Circuit World, Vol29 (2003).
- [2] A. Pohjoranta, R. Tenno, J.Electrochem.Soc., 154 (2007) D502
- [3]S. Yen, et al. Enhanced Uniformity of Pattern Copper Plating Process for Flip Chip substrate Microvia filling Application" IEEE Microsystems Packaging Assembly and Circuits technology Conference, IMPACT, (2014)
- [4]M. Lefebvre, et al. "Next Generation Electroplating Technology for High Planarity, Minimum Surface Deposition Microvia Filling" IEEE Microsystems Packaging Assembly and Circuits technology Conference, IMPACT, (2012)
- [5]K. Dietz, "Organic Additives in Copper Plating Baths (Part 1a)", CircuiTree, Feb 2000
- [6]K. Dietz, "Organic Additives in Copper Plating Baths (Part 2)", CircuiTree, Mar 2000
- [7]Y.M. Loshkarev, E.M. Gorova, "The Electrodeposition of Copper in the Presence of Brightening and Smoothing Agents", Protection of Metals, Vol 34, No. 5, 1998