@2017 IEEE. REPRINTED, WITH PERMISSION, FROM

A Novel Electroplating Technology with Leveling, Minimum Surface Deposition for HDI Application

Pei-Jung Wu†, Joanna Dziewiszek, Zukhra Niazimbetova‡, Ming-Yao Yen†, Dennis Yee *

Dow Electronic Material, The Dow Chemical Company

†No. 6, Lane 280, Chung Shan North Road, Ta Yuan Industrial Zone, Ta Yung Hsiang, Taoyuan Hsien, Taiwan, R.O.C.

‡455 Forest Street, Marlborough, MA 01752

* 15 On Lok Mun Street, On Lok Tsuen, Fanling, Hong Kong

IMPACT Conference Proceedings, October 2017.

ABSTRACT

Electrolytic copper micro via filling is an enabling technology, prominently used in today's manufacture of high density interconnect (HDI), to be driven by the needs for faster speed, smaller dimension and higher performance versus communication and electronic devices; and also in response to the evolution of the wafer manufacturing technology, which eventually required smaller and smaller pitch BGA substrate for packaging, more dense I/O counts increase transmission efficiency, and minimize routing reduce signals disturbance. Thus, the trend of circuits on HDI boards will tend to be constructed by high density stacked vias and smaller vias. And the increasingly difficult micro via geometries must be filled without void and skip plating over million vias, while maintaining plating rates capable of delivering production throughputs.

This paper describes the study on the factors affecting copper electroplating for micro via filling, and developing new plating formula with great surface leveling, thinner copper deposit thickness for direct current (DC) copper process for HDI application.

Introduction

Driven by the need for increased speed, portability and wiring density, the interconnect pitch on semiconductor packages and the corresponding High Density Interconnect (HDI) substrates continue to shrink. The combination of filled blind micro vias and build-up technology provides flexible routing to achieve higher wiring densities. With the rapid growth of this technology, the use of electrolytic copper for filling blind micro vias has become widely adopted process for manufacturing both HDI printed circuit boards and also semiconductor package substrates. The evolution of DC micro via filling systems over the past decade has seen substantial improvements in micro via filling performance. However, with the product application differentiation and technology development, the required plated copper thickness dropped from over 20 micrometer to values now close to 10 micrometer. And also, in order to reduce the risk of surface scratch mark, which caused by the equipment conveyor mechanism and thus impact the yield rate of subsequent etch process, the next generation of electrolytic copper plating process for HDI application are expected to have both via fill capability at thinner deposition thickness and excellent leveling properties.

Copper Electroplating

The vast majority of electroplating baths used in PCB fabrication are based on electrolytes composed of copper sulfate and sulfuric acid. Owing to the low cost and the convenient operation, these sulfates based systems area well-established technology, and have been widely used in the PCB industry for over fifty years.

Inorganic Components

There are three inorganic components in an acid sulfate electrolyte: copper sulfate is the primary source of cupric ions, sulfuric acid primarily accounts for solution conductivity, and chloride ion acts as a co-suppressor. For packaging substrate applications, a proper combination dedicate for micro via filling and uniform trace and pad profiles is critical.

Organic Components

Acid copper sulfate system operated without additives typically yield deposits of poor physical properties. Organic

additives, typically consisting of materials described as brightener, suppressors and levelers, are employed to improve grain refinement, throwing power, leveling and brightening of the deposit. What is more, some novel organic additives were developed to enable micro via filling behavior.

Suppressors, also referred to as carrier, are typically large molecular weight polyoxy-alkyl type polymers. Carriers are adsorbed on the copper surface to suppress the copper deposition rate, and the adsorption distribution is in concert with chloride ion.

Brighteners, also referred to as accelerators, are typically small molecular weight sulfur-containing compounds that increase the plating reaction by displacing adsorbed carrier. Brightener compounds may exist in several forms in electrolytic working baths.

Levelers are typically compounds with strong adsorption to copper surfaces, which greatly inhibit deposition rate. Such additives allow the deposition to progressively smooth the surface, by reducing the deposition rate in locations that receive higher fluxes of additive (such as protrusions).

Micro via filling can be considered an extreme form of surface leveling, in which leveler additives play critical roles in filling performance. In such systems, the deposition rate on entire surface of the PWB panel has to be suppressed in comparison to the deposition rate within the micro via.

Bottom-up Fill Mechanism

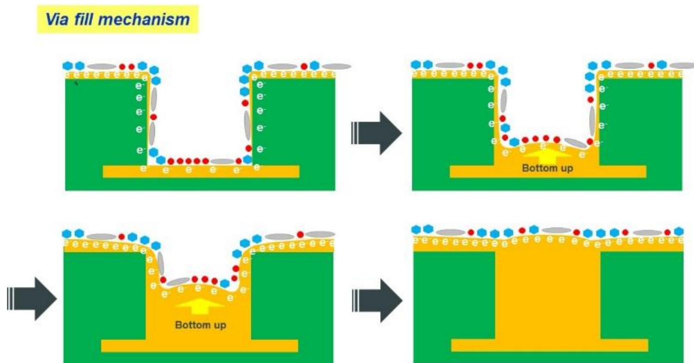

Figure 1. Via fill mechanism diagram

Bottom-up fill mechanism of micro via is achieved by this differential adsorption of additives at the surface and inside of the vias. In order to fill the vias with a high quality continuous copper deposit, the plating rate at the bottom of the vias must be substantially faster than that of the remaining areas, in order to avoid premature closure of the mouth of the via opening and the consequent formation of voids or seams.

Accelerated bottom-up filling has been attributed by the interaction of the organic additives system. The suppressor or carrier are adsorbed at high agitation regions and forms a current inhibiting film on the Cu surface. This film forms uniformly at all locations, assisted by the high solution concentration of suppressor. The accelerated bottom-up filling (i.e. “superfilling”) is driven by brightener concentration enhancement at the base of the feature (via or trench) during the plating process. Progressive reduction of surface area at via bottoms during deposition “squeeze” the brightener into ever decreasing area. This localized concentration of brightener further accelerates the plating rate relative to the surface. The leveler acts to suppress the plating at the corners of vias, and aid in reducing the formation of a void. In order to maintain bottom-up filling behavior, brightener concentration must be controlled within specified limits.

Production Equipment

With conventional vertical batch electroplating systems, increased production throughput may be realized by increasing the number and/or the size of the plating cells. When the size of a plating cell is increased, the number of panels within the cell increases proportionally. Unfortunately, increased panel loading tends to decrease plating uniformity, particularly when comparing panels from the center of the flight bar with those from the ends.

In contrast, the use of either horizontal or vertical conveyorized equipment promotes panel to panel consistency, as each panel “sees” the same overall flow and current distribution as it passes through the equipment. The improvements in consistency can be seen in both better surface thickness distribution and enhanced uniformity of throwing power and micro via filling, both within a panel and from panel to panel. Vertical In-line plating (VIL) systems have been shown to give plating uniformity ≤ 5.0% coefficient of variation (CV) across 18” x 24” panels.

However, when side to side variation within a panel is considered, vertical continuous systems hold a significant advantage over horizontal systems, in that only vertical systems allow the 2 sides of the panel to be processed in effectively identical physical environments. Vertical In-line plating equipment designs are particularly suitable for micro via filling applications, as the vertical panel orientation minimizes the air entrapment associated skipped or partially filled vias. In contrast, these defects can be problematic on the bottom side of panels processed in horizontal equipment.

Conveyorized systems have good uniformity and suitable design for micro via filling application than conventional vertical batch systems, but the panel guiding of conveyorized systems, such as the side guide and the bridge, will have the risk to scratch on the panel surface during the copper

electroplating. So then we will explore the factors affecting micro via filling and scratch mark of copper electroplating.

Impact of Mass Transport and Current Density

Mass transport and current density has a significant impact on via filling capability. To make a correct selection of these parameters will widen the range of micro via dimension and aspect ratio that can be produced by a single process chemistry. To understand how to best exploit these parameters, extensive testing to characterize the effects of solution agitation and current density on via filling was conducted.

Based on the test result of solution flow rate effect (Figure 2), filling performance are not much different whether it is high or low levels of solution flow rate in small dielectric side. In contrast, for the thicker dielectric layer, high flow rate will contribute to the mass transfer of copper ions to enhance micro via filling performance.

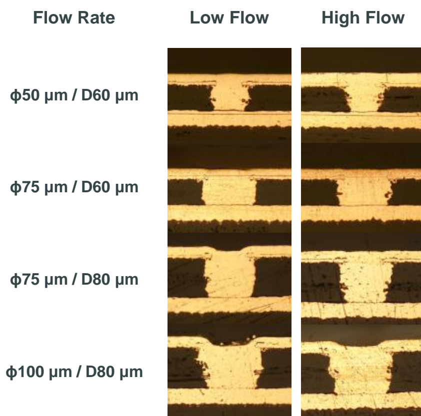

Figure 2. Micro via fill performance as function of solution flow rate (at 15ASF and 15µm copper thickness)

Figure 3 and 4 are the via filling and scratch mark performance as a function of current density. Higher current density was found to enhance via filling performance, particularly in large diameter vias (100µm or above). However, this improvement comes at the price of increased risk of improperly filled smaller diameter vias (less than 75µm). At high current density, the curvature enhanced accelerator coverage (CEAC) mechanism is no longer followed, improper fill may lead to defects ranging from "seams" within the plated deposit, to completely voided vias.

For scratch mark testing, regardless of the level of current density, the scratch mark can't be improved (Figure 4).

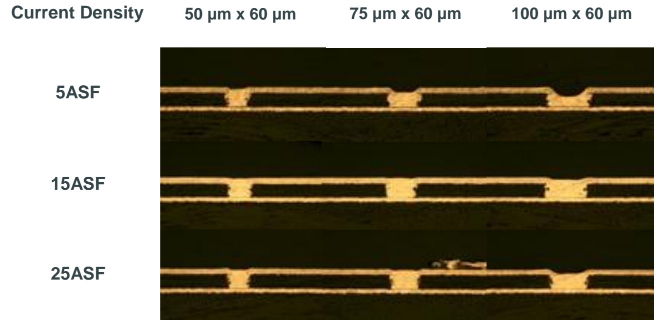

Figure 3. Micro via fill performance as function of Current Density (at 15ASF and 10µm copper thickness)

Current Density	5ASF	15ASF	25ASF
Scratch mark deep	2.8µm	3.8µm	3.6µm

Figure 4. Scratch mark performance as function of Current Density

Impact of copper sulfate concentration

A typical acid sulfate system contains copper sulfate, sulfuric acid and chloride ion. As the primary source of cupric ions, concentration of copper sulfate is important on the mass transfer, and thus affect the micro via filling performance. Figure 5 shows the effect of copper sulfate concentration on micro via filling performance, it can be seen that copper sulfate concentration greater than 200g/L is used to achieve good micro via filling performance, significant improvement will be found especially in large diameter (100µm or above).

For scratch mark testing, the change in copper sulfate concentration did not improve significantly for scratch mark performance (Figure 6).

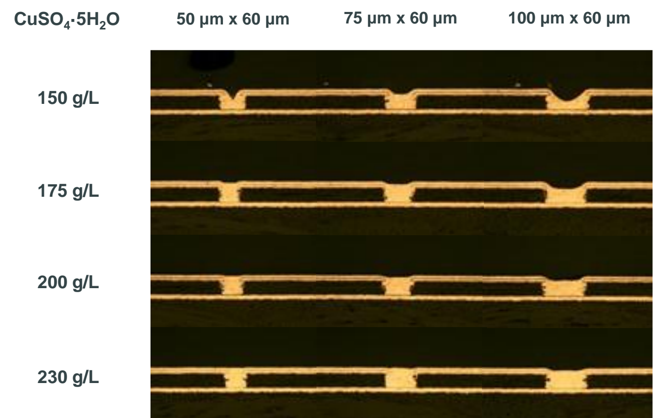

Figure 5. Micro via fill performance as function of CuSO4·5H2O concentration (at 15ASF and 10µm copper thickness)

$CuSO_4 \cdot 5H_2O$	150 g/L	175 g/L	200 g/L	230 g/L
Scratch mark deep				
	2.9µm	2.6µm	3.4µm	3.8µm

Figure 6. Scratch mark performance as function of $CuSO_4 \cdot 5H_2O$ concentration (at 15ASF)

Impact of Organic additives

The excellent additive systems for acid copper sulfate bath developed in the 1960s successfully produce bright copper deposits with smooth surfaces and high ductility. Since then, the evolution of a wide range of copper electroplating applications have been accompanied by the development of various types of additives.

In Figure 7, we compared micro via filling performance and mechanism of three distinct formulations as a function of copper deposition thickness. Formula A shows a super-filling mechanism in which micro vias are filled at 10µm deposition thickness; but this formulation has the risk of void, since the copper deposition rate on via bottom are lower than corner. In contrast, the filling mechanism of Formula C will improve void issue, but this formulation must be deposited with a thicker copper deposition thickness to fill the micro via.

THK	Formula A	Formula B	Formula C
5µm			
10µm			
15µm			
20µm			

Figure 7. Micro via fill performance as function of copper deposition thickness at CD 15ASF (100µm diameter x 60µm deep via)

From scratch mark test result, the design of the formula for scratch mark performance improving has a significant contribution. As a result in Figure 8, Formula C shows a lower sensitivity on scratch mark performance, the deep of scratch mark is 1.7µm. From the result of electrochemical analysis in Figure 8, the time required for Formula A to reach a stable potential will be longer than Formula C. When the time required for the additive to balance is longer, the adsorption of the additives on the panel surface will be unstable, resulting in different in deposition thickness.

Formula	A	B	C
Appearance			
Scratch mark deep			
	4.4µm	3.5µm	1.7µm

Figure 8. Scratch mark performance as function of formula (at 15ASF)

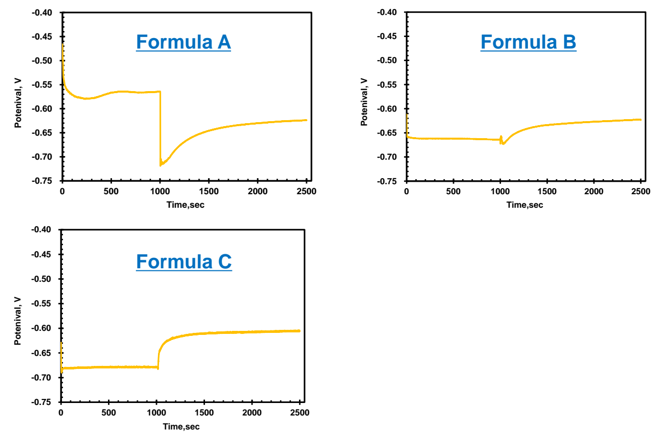

Figure 9 Galvanostatic measurement as function different formula.

According to the via fill and scratch mark test results, we found that the design of the formulation and additives are critical to achieving good micro via filling and scratch performance. Based on the study results, we are developing a new formula which shows good micro via filling performance and scratches performance.

Dielectric 60µm	ϕ50µm	ϕ75µm	Scratch mark
Via fill performance			
	ϕ100µm	ϕ125µm	
			Scratch deep
			1.8 µm

Figure 10 Micro via fill and scratch mark performance of new formula.

Summary

Evolution of DC micro via filling systems over the past decade has shown substantial improvements in micro via

filling performance. However, driven by the evaluation of product applications and technologies, the required plated copper thickness dropped from over 20μm to values close to 10 microns. And also in order to reduce the risk of surface scratch mark caused by the equipment, the next generation of electrolytic copper plating process for HDI application are expected to have both via fill at thinner deposition thickness and excellent leveling properties.

This article is a study on the factors for micro via filling and scratch mark; from the test results, the way to achieve these two requirements only through a new formula design. We are developing new plating formula with great surface leveling, thinner copper deposit thickness for direct current (DC) copper process for HDI application.

References

1. W.P. Dow, H.H. Chen, M.Y. Yen, C.W. Liu, *J. Electrochem. Soc.*, 2(6) 259-267(2007).
2. T. P. Moffat, D. Wheeler, and D. Josell, Journal of The Electrochemical Society, C262-C271, 151, (2004).
3. J. P. Herty, D. Pletcher, and T.H. Bailey, Journal of Electroanalytical Chemistry, 338, 25 (1998)
4. M. Lefebvre, E. Najjar, L. Gomez, L. Barstad, “Next Generation Electroplating Process for HDI Microvia Filling and Through Hole Plating”, circuit board technologies technical communications, IMPACT, (2008).
5. T. P. Moffat, D. Wheeler, and D. Josell, *The Electrochemical Society Interface*, p. 46, 2004