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Interconnect Material Total Solutions for Advanced Packaging Substrate Applications

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ABSTRACT

With the advancements in artificial intelligence (AI), machine learning (ML), and 5G networks, data generation grows by over 20% [1] each year. The rapid growth of data will undoubtedly require the upgrade of existing networking, data processing, and storage infrastructures, which means more high-speed and high-frequency devices are needed. Over the past decades, packing substrate evolved to bridge the gap between the chip and printed circuit board to meet such needs. Miniaturization, greater integration, and higher performance are the critical technology directions for advanced substrate development. Many companies invested in the advanced substrate to meet the global market demand. In recent years, DuPont Interconnect Solutions (ICS) business has invested in developing advanced materials for the Integrated Circuit (IC) substrate and launched innovative substrate full-process solutions. This paper will introduce DuPont's product portfolio, process capabilities, and dive deep into advanced SAP desmear, electroless Cu, electroplating and via filling Cu chemistry, and fine line dry film photoresist products.

INTRODUCTION

Integrated Circuit substrates are crucial to bridge IC chips and Printed Circuit Boards (PCB). Since the electronics industry adopted the IC substrates a few decades ago, it has been used in many applications, including personal computers, smartphones, high-performance computing (HPC), and other electronic systems. The substrate technology has evolved from early on lead frame, wire-bonding Ball Grade Array (BGA), and Chip Scale Packaging (CSP) to Flip Chip (FC) BGA, FCCSP, and even more advanced technologies such as CoWoS, Embedded Die in IC substrate, etc. [2]

Today, information forms the foundation of our connected world. The electronics industry has experienced a transformation over the past years, driven by the increasing demand for smarter and more advanced devices. The data explosion will certainly overwhelm existing networking, data processing, and storage infrastructures. The surging demand in HPC, data centers, and 5G networks drove the IC substrate Compound Annual Growth Rate (CAGR) of over 20% from 2019 to 2022 [3]. Advancements in artificial intelligence (AI), machine learning (ML), and autonomous driving are expected to be the next wave of advanced IC substrate growth engines. These new applications bring more technology development needs for advanced substrates. Innovations are required to solve the challenges of achieving high performance, high integration, yield, miniaturization, reliability, and cost targets while maintaining sustainability standards. Many investments have been made through the IC substrate ecosystem to solve these challenges. This paper will introduce the IC substrate full-process solutions developed at DuPont's ICS business.

DUPONT'S IC SUBSTRATE SOLUTIONS

Product Portfolio and Process Capabilities

As CMOS scales to more advanced nodes, advanced packaging substrates become critical to get more performance out of a device through 2-dimensional structures for advanced applications. There are many technical challenges to meeting high-performance needs, including fine pitch interconnection, improved electric performance, higher power consumption, thermal management, and warpage control from larger package sizes. The need to integrate diverse functionalities into ever-smaller devices creates a new value proposition for advanced substrate technologies that innovations need to be achieved through the whole value chain. DuPont has long been a market leader in high-performance, high-reliability materials for demanding applications. The broad product portfolio makes it possible for DuPont to bring all different elements together for the advanced substrates.

Figure 1 is DuPont's IC substrate offering chart. A broad spectrum of solutions from dielectrics, metallization chemistries for electroless Cu, redistribution layer (RDL) electroplating Cu, Copper pillars, and solder bumps to dry film imaging photo-resist (PR). Materials designed to work in concert make a significant impact on device performance and reliability. A few newly developed metallization and imaging materials will be introduced in the following materials session.

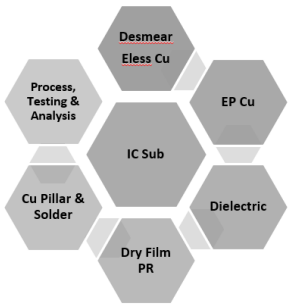


Figure 1. DuPont's Advanced Substrate Solutions

Materials and processes both play significant roles in electronic device manufacturing. Unlike the semiconductor front-end processes, where the world-class fabs are leading the process development effort, back-end processes such as advanced IC substrates and PCBs require material suppliers, equipment vendors, and substrate fabs to work together to develop the technology. DuPont has invested in a wide range of process capabilities in substrate technology. Figure 2 shows the process capabilities, including tools from vacuum laminators, laser & mechanical drilling, Eless Cu plating, imaging tools, various EP Cu plating tools, and advanced testing and analysis equipment. DuPont's broader materials portfolio and the differentiated process infrastructure enabled rapid formulation iteration focus and performance & processability validation.

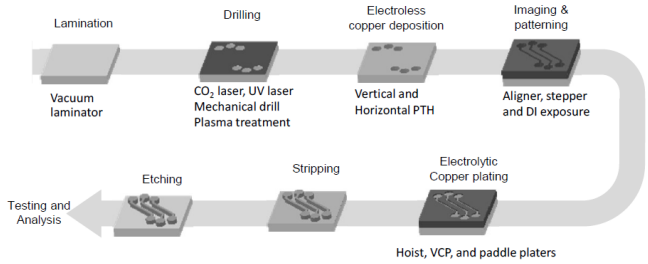


Figure 2. DuPont's Process Capabilities

Metallization materials

Copper plating, including electroless Cu and electroplating Cu, has been used in the electronic industry for over half a century. Assembling multiple chips in multiple layers requires more electrical connections, which in turn requires both thinner lines within the Redistribution Layer (RDL) and a more complex design. The performance and characteristics of the materials and processes applied significantly impact the ability to achieve such high integration reliably.

One of the challenges in the FCBGA manufacturing process for high-speed and high-frequency (HSHF) applications is adhesion. As the dielectric materials change to more hydrophobic to meet the low loss requirements, achieving adhesion between the Cu layer and the dielectric in a smoother interface becomes challenging. DuPont's newly developed Circuposit™ SAP8000 product is designed to solve such challenges. Table 1 lists the key properties of Circuposit™ SAP8000 product and Figure 3 shows it delivers >90% throwing power performance for a 40 µm via.

Table 1 Circuposit™ SAP8000 product performance summary

CTQ		Existing product	SAP8000
Plating thickness		~0.50 µm /15 min	~0.35 µm / 15 min
Throwing Power		80%	90%
Peel strength (kgf/cm)	GL107	0.34 ± 0.02	0.43 ± 0.02
	GL102	0.35 ± 0.03	0.43 ± 0.03
	GXT62	0.45 ± 0.08	0.68 ± 0.09
	GX92	0.79 ± 0.05	0.81 ± 0.07
Blister		Blister Free	Blister Free
Dry film adhesion		10/10 µm pass	10/10 µm pass
QVP-via break point Test		0 fail	0 fail
EOL test with TCT		<2%	<2%
E'less Cu bath life		1 week	1 week (2 m^2/L)

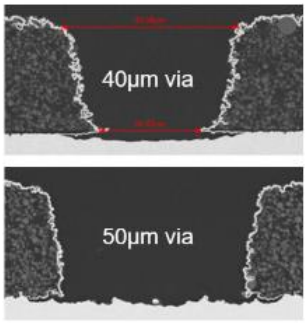
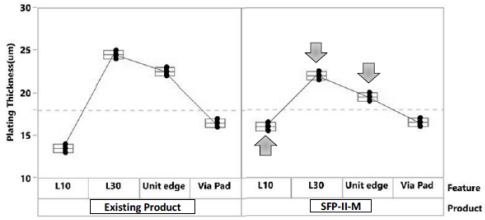


Figure 3: Circuposit™ SAP8000 product uniform Eless layer with >90% throwing power

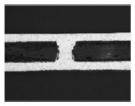
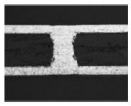
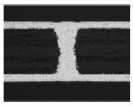
Another challenge in the advanced substrates manufacturing process is good via-filling performance and pattern plating uniformity for electrodeposited Cu, which is critical for downstream process and reliability. Plating additives help control the topography of the structures being plated. However, for most additives, there is a trade-off to achieve via filling and uniformity, so accommodating both properties is extremely difficult. DuPont's recently commercialized Microfill™ SFP-II-M solution shows a good balance of achieving both targets. This product also demonstrates good through-hole filling capability at the CSP core layer. Tables 2 and 3 show the performance summary and cross-section of the Microfill™ SFP-II-M product in the CSP core layer. Since the launch of the product, SFP-II-M has gained multiple Process of Records (PORs) at various leading IC substrate customers and demonstrated reliable performance.

Table 2 Microfill™ SFP-II-M product performance summary



Chemistry	Existing Product	SFP-II-M
Conditions	20ASF, 42min	
L10(Trace)	13-14	15.5-16.5
L30(Dense line)	24-25	21.5-22.5
Unit edge	22-23	19-20
Via pad(Unit center)	16-17	16-17
Unit-R(um)	10.5-11.5	5.5-6.5
Via FillingΦ70um	+2~3	-1~-2

Table 3 Microfill™ SFP-II-M product CSP core layer performance summary

Dielectric	60µm	100µm	150µm
Diameter	60µm	80µm	80µm
Neck	60µm	60µm	60µm
X-section			
Via-filling	Dimple=1.5µm	Dimple=1.6µm	Dimple=1.9µm

Imaging materials

Fine-line patterning requires dry-film photoresists and resist strippers that accommodate shrinking dimensions and enable high-quality traces. These patterning process steps are essential for high-speed circuit performance. The photoresist patterning is critical because it directly affects the precision of which Cu lines can be deposited. Better adhesion, resolution, and chemical resistance performance are keys to creating Cu traces with well-defined line widths and clear, sharp sidewall profiles, which are important for signal transmission.

DuPont has long been an industry leader in dry-film photoresists and continues to develop new products in its Riston® family of resists. In recent years, two different types of imaging solutions, stepper, and laser direct imaging (LDI) solutions, have been developed for fine-line FCBGA and FCCSP applications.

Riston® DI1600 is the advanced H-line direct imaging fine Line Solution with wide operation latitude and high productivity through fast photo speed and stripping time. It can achieve 5µm resolution and adhesion at 25µm thickness on T5 copper foil and ABF GX-T31 substrates and 4 µm resolution and adhesion at 15µm thickness using the ORC Fdi-3 imaging tool. DI1600 has demonstrated reliable plating performance and a straight Cu trace profile with DuPont plating solutions.

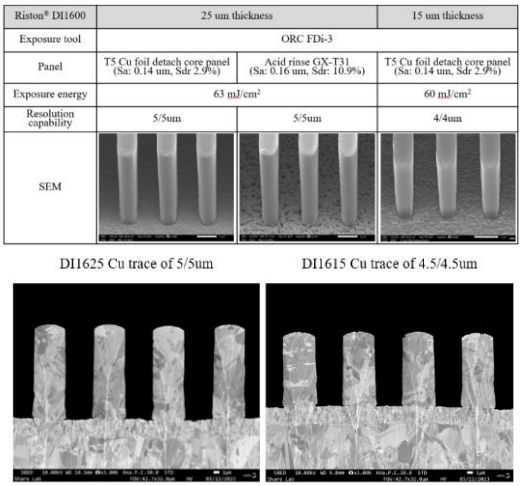


Figure 4: Riston® DI1600 product resolution and plated Cu traces

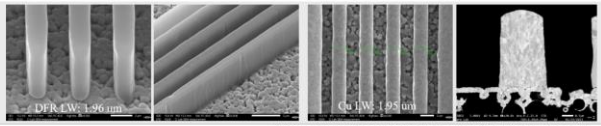
Figure 4 shows the resolution capability and deposited Cu trace profile with DuPont Microfill™ SFP-II-M plating solution. Table 4 shows the 100% open/short yield at 4 µm fine lines.

Table 4 Riston® DI1600 product pass rate of Open/Short Yield at 4 µm

Exposure Energy (mJ/cm²)			50	60	70
Offset (um)			-1.5	-1.5	-2.0
Resolution	L/S=4/4	ADI actual space (um)	3.84	3.27	3.63
		O/S yield	100%	100%	100%
	L/S=5/5	ADI actual space (um)	4.70	4.13	4.41
		O/S yield	100%	100%	100%
Adhesion	L/S=4/12	ADI actual width (um)	3.20	3.87	3.48
		O/S yield	100%	100%	100%
	L/S=5/15	ADI actual width (um)	4.27	4.87	4.60
		O/S yield	100%	100%	100%

DuPont also developed a stepper fine line imaging dry film photoresist to accommodate customers' tool preferences. Riston® SD2007 is one of the newest developed imaging solutions that can achieve 2µm resolution capability and a smooth sidewall profile using both stepper and LDI tools. Table 5 shows the SD2007's 2um line/space after stripping Cu profile on ABF GL102. Such fine structure performance will enable the packaging substrate for more advanced applications.

Table 5: Riston®SD2007 Dry Film Resist (DFR) performance

DFR	SD2007
Substrate	0.3um E'less Cu on GL102 (Sa 0.05 um)
Exposure	Ushio UX-23101 (UPL-101), I-line, Dose 135 mJ / Focus 0 µm
Development	Min. Dev. Time: 10 s; BP 30%; Total Dev. Time: 33 s
	ADI – DFR Profile / ASI – Cu Top View and Profile
Pitch 4 µm Positive tone	

*ADI: after development inspection; ASI: after stripping inspection

CONCLUSIONS

Building infrastructures for a connected world needs advanced interconnect for the future generation of electronic devices. There is a great need for broad collaboration in technology, design, standardization, and supply chain development to enable the advanced IC substrate. With more than half of a century's technology development in metallization, Imaging, dielectric, and recent investment in the advanced substrate, DuPont is advancing to be an integrated total solution provider and partner of choices for customers to solve the challenges in advanced interconnect.

REFERENCES

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[2]. Advanced Chip Packaging: How manufacturers can play to win, Ondrej Burkacky, Taeyoung Kim, and Inji Yeom, May 24, 2023, McKinsey & Company

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