I/O Decoupling in High Speed Packages Using Embedded Planar Capacitors

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Abstract

Embedded passives are gaining in importance due to the reduction in size of consumer electronic products. Embedded passives are gradually replacing discretes due to the miniaturization of electronic products. Integration of these passives within the package increases the real estate for active components. This would increase the functionality of the system. Among the passives, capacitors pose the biggest challenge due to the large capacitance required for decoupling high performance circuits. This paper will highlight the performance of DuPont's planar embedded capacitor laminates in organic packages to provide I/O decoupling for active circuits.

1 Introduction

Miniaturization of electronic products due to the current trend in the electronic industry has led to the integration of components within the package. Traditionally, discrete decoupling capacitors placed on the surface of the board or the package have been used to decouple active switching circuits. [1-4] However, with an increase in the clock rates and its harmonics with technology nodes [5], decoupling has to be provided in the GHz range. Discrete decoupling capacitors are no longer effective in this region because of the increased inductive effects of the current paths of the capacitors, which limits their effectiveness in the tens of MHz range.[6] Inclusion of embedded planar capacitor laminates in the stack up have shown improvements in the overall impedance profile and have been shown to exhibit better noise performance[7,8]. The main contributor to the superior performance is the reduced inductive effects of the power-ground planes because of the thinner dielectrics of the embedded laminate.

In this paper we investigate the performance of various embedded planar capacitor laminates in decoupling I/O circuits. The contributions of this paper are as follows: (a) Demonstration of noise coupling suppression between signal traces and power-ground planes. (b) Eye diagram simulations for different interconnect configurations and embedded planar capacitor laminates.

The paper is organized as follows: Section 2 of the paper will describe the design of the active test vehicle to capture the simultaneous switching noise phenomenon because of the I/O return current path. In Section 3, simulations will be shown for high speed buses with single ended and differential I/O's at data rates of 1Gbps, 5Gbps and 10Gbps. The performance comparison of different embedded planar capacitor laminate layers will be done by comparing the eye diagrams.

2 Noise Coupling Suppression between Signal and Power Ground plane

A detailed analysis into the coupling between the signal trace and the power-ground plane of the stack up is done in this section. The measurement set up, modeling technique and model to measurement correlation of the results are presented. The cross section of the stack up with the excited signal trace (SIG) is show in Fig. 1.The signal trace is excited from the surface at the first probe point (SIG probe-point). The transmission line test vehicle was designed such that the signal via passes through the planar capacitor laminate layer onto the signal trace SIG. The signal trace extends for five and half inches across the board and all the ground planes in the stack up are tied to one another by through vias. The signal trace SIG has a stripline configuration and has a characteristic impedance of 50Ohms. The trace is referenced to a power and ground plane as seen in Fig. 1 and the load end of the signal trace is left unterminated. The second probe point (P-G probe point) was defined on the power-ground plane and was defined as the receiver port. The measurements were done for 3 planar capacitive laminate materials embedded in them, a 50um micron thick FR-4 and 18um and 25um thick HK04 polyimide dielectrics.
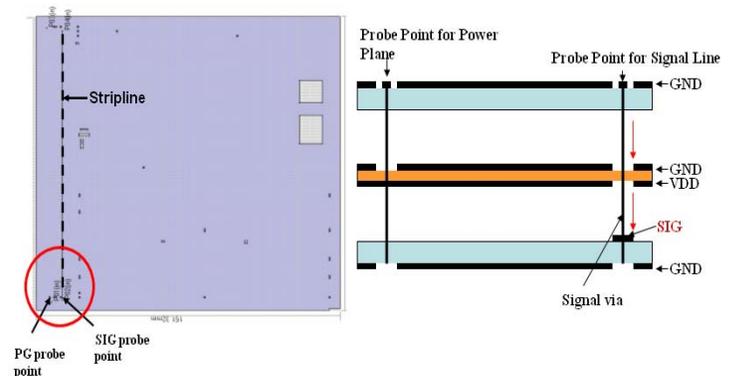

Fig. 1: Cross section of the signal to power-ground coupling experimental set up.

The measured coupling results between port1 and port2 (S21) are plotted for all 3 cases in Fig. 2. The results clearly show that the energy coupled from the signal trace to the power-ground plane is the least in the case of the 18um thick dielectric. In the following, the modeling technique used to capture the effect of the signal coupling to the power-ground planes and model to hardware correlation of the measurement will be shown.

a) Modeling of signal to power-ground plane coupling
The modeling technique used in the analysis will be briefly described in this section. The modeling technique has to be able to capture the voltage fluctuations between the power-

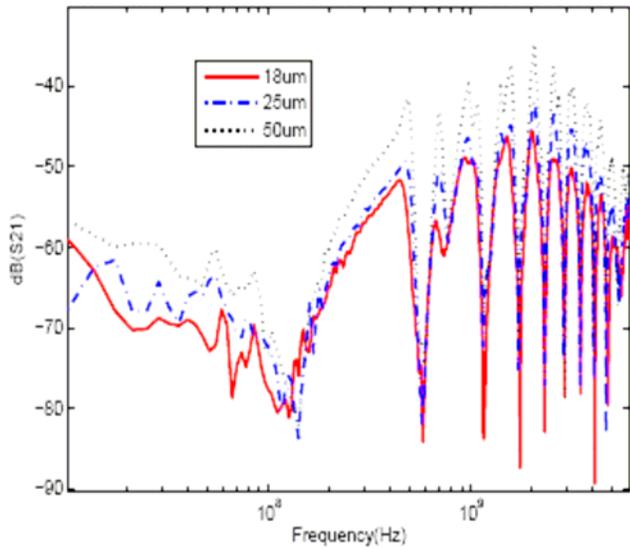ground plane. A stripline model has been proposed in [9], which was used in this paper.

Fig. 2: Signal to power- ground coupling for all dielectrics.

An equivalent multiport model of the stripline is shown in Fig. 3. Z_{par}^c and Z_{str}^c represent the characteristic impedance of the parallel plate and stripline modes, respectively. The controlled sources represent the coupling between the two modes and can be obtained from the dielectric thicknesses.
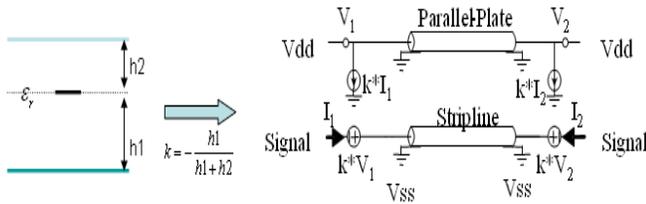

Fig. 3: Equivalent model of a stripline

The stripline SIG was designed to be a 50Ohm line, the thickness of the dielectric in which the stripline is embedded is 16mils thick and has a dielectric constant of 3.5, which results in a line width of 7.1mils for the transmission line. The transmission line is placed at the center of the 16 mil thick dielectric. Since the ground planes are tied together using vias, the effect of the parallel combination of all the power ground pairs needs to be taken into account. The thickness of the dielectric in which the stripline is embedded is 16mils (406.4um) as compared to the 18um, 25um and 50um thick planar dielectric layers. The dielectric constant of both materials are comparable and since they are in parallel, the capacitance of the thinner power-ground layer will dominate. The input parameters to the power plane were obtained by modeling the power-ground plane pair using the transmission matrix method. A total of 3 ports were defined in the model at the input, output and power-ground probe locations corresponding to the similar locations on the planes. The S parameter frequency response of the 3 ports were used as the

input to the model, which was simulated using ADS. The signal via transitions from the top surface of the board to the SIG layer through the embedded capacitor laminate layer. The coupling from the signal trace to the power-ground planes as obtained with the model and measurement for the 18um thick embedded capacitor laminate layer is plotted in Fig. 4. The modeled to measured result shows good correlation over the frequency band of interest. As shown in the previous section, the measured results of all 3 capacitive layers are plotted in Fig. 2 and it can be clearly seen that the 18um thick dielectric provides the best isolation between the signal and the power-ground probe point.
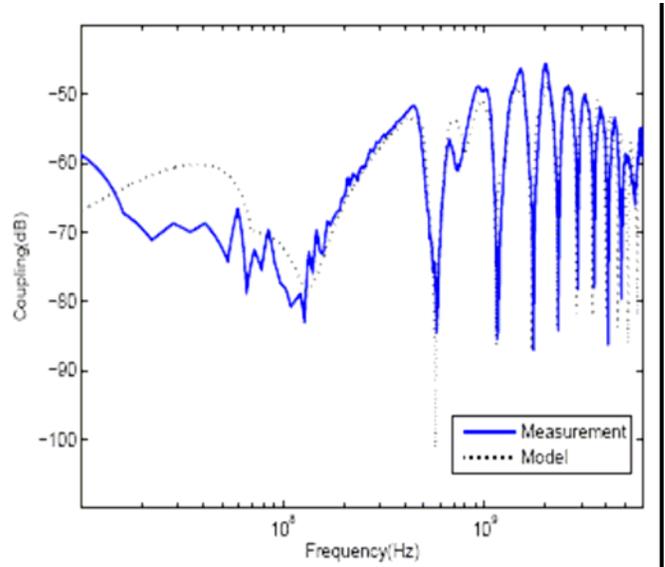

Fig. 4: Modeled to measured coupling between signal trace and power-ground planes for the 18um thick dielectric.

b) Active test vehicle

An active test vehicle was designed using the embedded capacitor laminate layers to investigate their performance in the time domain. The test vehicle consisted of a clock generator, transmission lines, termination resistors and probe points to measure the power-ground noise as well as the clock signal.

The cross section of the active test vehicle showing the signal path is shown in Fig. 5. The test vehicle consists of 2 stripline configurations. The upper SIG layer has 2 ground planes as its reference planes while the bottom SIG layer has a power and ground plane as its references as shown in Fig. 5.
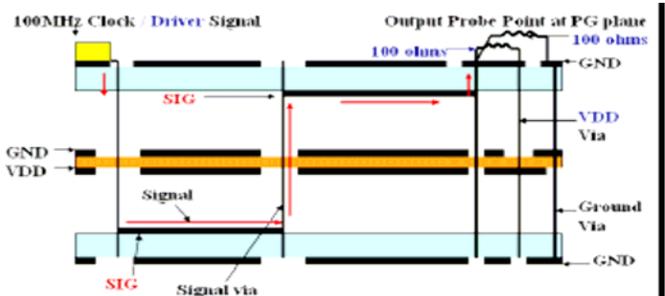

Fig. 5: Cross section of the active test vehicle

The length of the transmission line from the driver to the termination resistor is 20inches and the width of the reference planes are 1inch. A 100MHz clock oscillator was used as the input excitation signal. The transmission line on the signal trace was designed to be 50Ohm . The dielectric constant and the thickness in which the transmission lines were embedded were identical (i.e, the thickness and dielectric constant of the material were 16mils and 3.5 respectively). The width of the transmission line was 7.1mils and the thickness of copper on all planes was 1.4mils. The test vehicle was powered at 3.3V by connecting it to a power supply using an SMA connector. The active test vehicle included 2 decoupling capacitors of values 0.1uF and 0.01uF as specified in the data sheet for the clock oscillator. The transmission line was terminated with 2 100Ohm resistors connected to the power and ground plane respectively to give an equivalent termination resistance of 50Ohm. Probe points for a passive probe were defined along the length of the transmission line to measure the power-ground noise that was generated due to the return current issue. An SMA connector was connected at the load end of the transmission line to measure the power-ground noise. The equivalent model of the cross section of the active test vehicle is shown in Fig. 6.
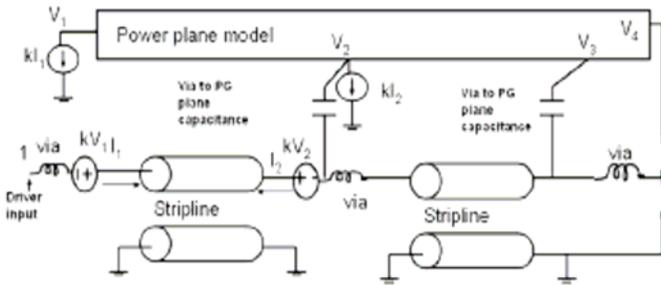

Fig. 6: Equivalent model of the signal configuration of the active test vehicle

As mentioned previously, the input excitation waveform was a
100MHz clock. The driver model to simulate the clock oscillator was developed by using a combination of switching resistors. One end of the driver model was connected to the V_{DD} plane while the other was connected to the ground plane. The driver acts like a voltage divider and the output of the model is fed as the input to the transmission line model. The input parameters to the switching resistors are the rise, fall and time period of the 100 MHz clock. The model to measurement correlation of the input pulse is shown in Fig. 7. The spike observed in the measured result is due to the loop inductance of the signal-ground loop in the passive probe used to probe the output pin of the clock oscillator.
The model included the via inductance from the top surface to the bottom SIG layer, the via inductance between the 2 signal layers and the via coupling between the signal via and the power-ground plane. The measurement was done by connecting a cable to the SMA connector, which connects to the power-ground plane at the load end. The other end of the

cable was attached to the input of a HP 54615B 500MHz oscilloscope with a sampling rate of 1GSa/s. The model to measurement correlation for the switching noise with the 18um thick dielectric is shown in Fig. 8.
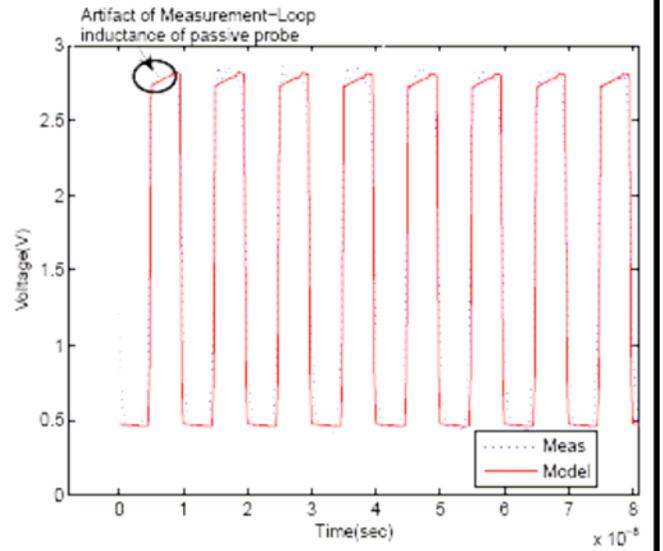

Fig. 7: Model to measurement correlation of the input waveform.
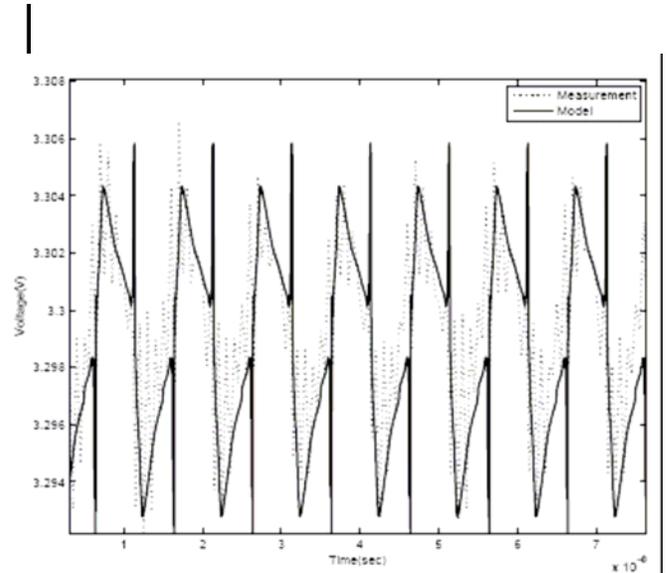

Fig. 8: The model to measurement of the noise waveform for 18um thick dielectric.

The peak-peak noise voltage is 15mV and is captured by the model. The measured noise comparison for all 3 dielectrics is plotted in Fig. 9. The noise voltages for the 18um, 25um and 50um dielectric are 15mV, 18mV and 37mV respectively. The decrease in the noise waveform magnitude can be explained as follows: The thin dielectrics have a two fold advantage, the capacitance of the structure increases for the same dielectric as given by (1)

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} \tag{1}$$

where, ε_r is the relative dielectric constant of the

dielectric, A is the area of the capacitive structure and d is separation between the plates of the structure. Also, the inductance of the same structure, which is given by (2) reduces due to a decrease in the separation between the plates.

$$L = \mu_o d \qquad (2)$$

The effective increase in the capacitance and decrease in the inductance leads to an overall decrease in the impedance of the power planes as given by (3)

$$Z = \sqrt{\frac{L}{C}} \qquad (3)$$

Electromagnetic waves propagating through the power-ground plane will see a reduced impedance, therefore generating less noise voltage as per ohms law.
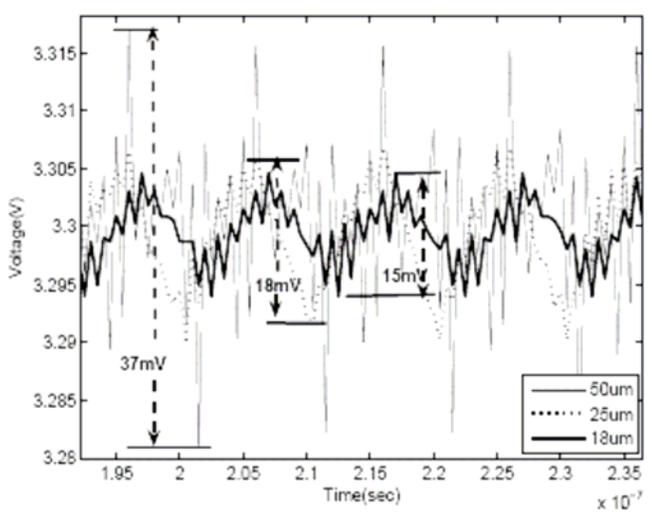

Fig. 9: Noise voltage comparison for the 3 dielectrics.

The normalized noise voltage with respect to the thickness is plotted in Fig. 10. The model and the measured results agree very well. The modeled result is plotted as a straight solid line and the measured result is plotted as a circle.
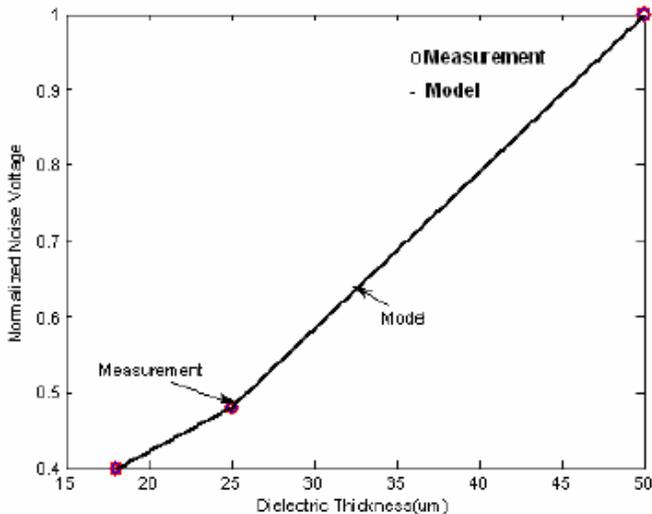

Fig. 10: The modeled and measured normalized noise voltage.

3 SSN and Eye Opening Simulations

This section describes the different simulations performed for single and differential bus configurations for data rates of 1Gb/s, 5Gb/s and 10Gb/s. The transmission lines in these simulations were in the stripline configuration and were terminated differentially with matched loads.

The first configuration was a 16 bit Front Side bus (FSB). This configuration consists of 16 50Ohm uncoupled single ended transmission lines terminated differentially at the load end with 2 100Ohm resistors to give an effective termination of 50Ohm. The model used in this simulation was similar to the stripline model used in the transmission line test vehicle. The length of transmission line is 200mm and the dimensions of reference planes were 200mm by 200mm. The methodology used to carry out the simulations was similar to the method mentioned in the previous sections. The simulation set up is shown in Fig. 11. The different dielectric layers used in the simulations are listed in Table 1.
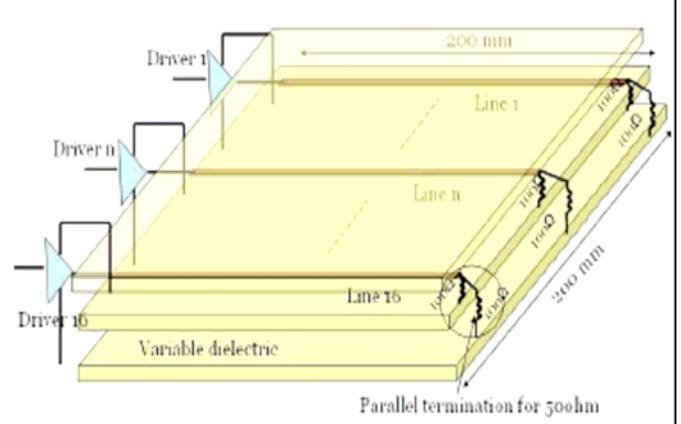

Fig. 11: Simulation set up for the 16bit FSB.

Table 1-Dielectrics used in the SSN and Eye Opening Simulations.

Dielectric thickness(um)	Dielectric constant	Loss Tangent
8	3.5	0.003
12	3.5	0.003
18	3.5	0.003
25	3.5	0.003
50	4.2	0.015
50	3.5	0.008

The simulation for the FSB was done with pseudo random bit stream sources (PRBS) at 1Gb/s. The rise and fall times of the source was 200psec with a 1V voltage swing. The driver model used was similar to the driver models used in the active test vehicles. The variation in the SSN is listed in Table 2. The last row in Table 2, refers to the case where a simulation was carried out with the 50um thick dielectric, with a dielectric constant of 3.5 and 100 decoupling capacitors with C=100nF, ESR=0.03Ohm and ESL=400pH scattered around the driver end, receiver end and along the length of the transmission line. The effectiveness of the different planar capacitor laminate can be compared by their eye diagrams. Fig. 12 and Fig. 13, compare the eye diagrams of the last 2 rows of Table 2 respectively. The improvements in the eye diagrams are evident with the decoupling capacitors.

Table 2- SSN variation with different dielectrics at 1Gb/s

Dielectric thickness(um)	Dielectric constant	SSN peak to peak magnitude(mV)
8	3.5	237
12	3.5	414
18	3.5	445
25	3.5	489
50	4.2	968
50	3.5	980
50 + 100 × 100nF decaps	3.5	695

However, the performance improvement can be enhanced considerably when a 18um thick dielectric with a dielectric constant of 3.5 is used as shown in Fig. 14. From the above results it can be inferred that for decoupling I/O circuits planar embedded capacitor laminate can be more effective compared to using discrete decoupling capacitors.
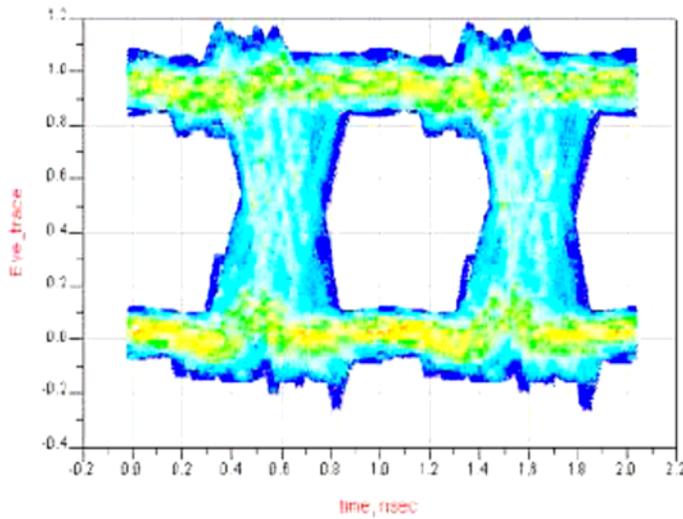

Fig. 13: Eye diagram result for the 50um planar capacitor laminate with 100 decoupling capacitors at a data rate of 1Gb/s.

Fig. 12: Eye diagram result for 50um dielectric planar capacitor laminate with a dielectric constant of 3.5 at a data rate of 1Gb/s

Fig. 14: Eye diagram result for row 18um dielectric planar capacitor laminate at a data rate of 1Gb/s.

Similar analysis was done for a 4 pair differential microstrip configuration. The simulation data rates used were 5 Gb/s and 10 Gb/s with PRBS input waveforms having a voltage swing of 1V. The rise and fall times for a 5 Gb/s driver model were 40psec with a skew of 10psec between the 2 differential signals. The common mode and differential mode resistance of the transmission lines were 50Ohms and 100Ohms respectively.

The simulation set up for the 10 Gb/s was identical with the previous case, the difference being in the rise time and fall times. The rise and fall time were 20psec each and the skew between drivers of each differential pair was the same as for the 5 Gb/s (i.e 10 psec). The SSN was much less than the single ended as would be expected for a differential driver set up and the eye diagrams are much cleaner as shown for the 18um dielectric and 50um dielectric with a dielectric constant of 3.5 each in Fig 15 and Fig 16 respectively for a data rate of 10 Gb/s. The simulation results are tabulated for the different dielectrics in Table 3.
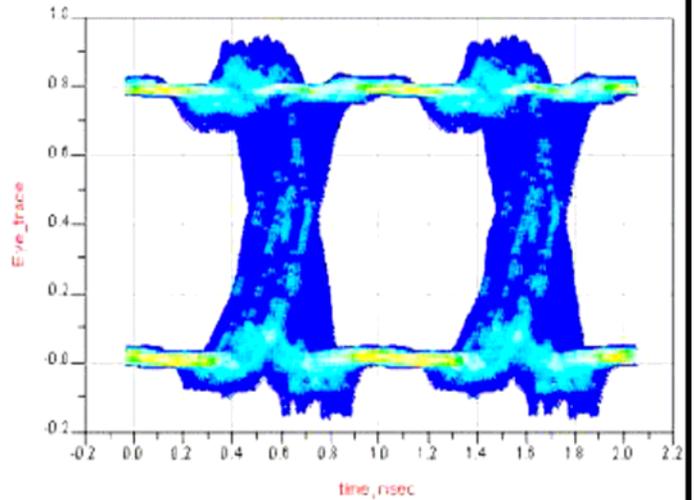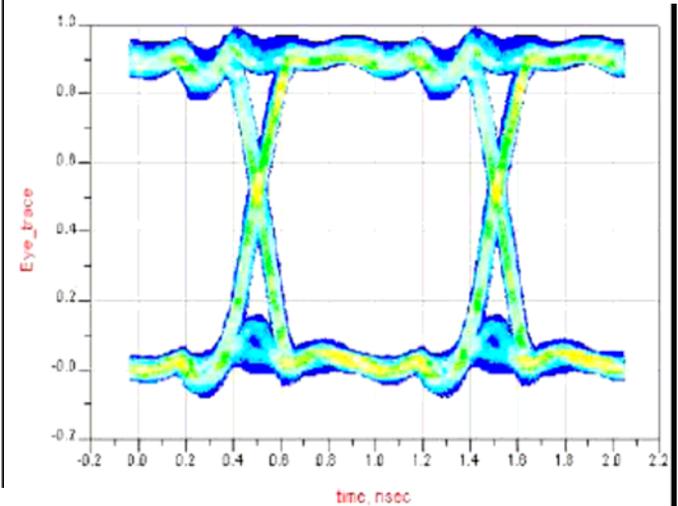
Table 3- SSN variation with different dielectrics at 5Gb/s and 10Gb/s for a 4 pair differential microstrip configuration.

Dielectric thick-ness(um)	Dielectric constant	SSN peak to peak magnitude(mV) at 5Gb/s	SSN peak to peak magnitude(mV) at 10Gb/s
8	3.5	8	44
12	3.5	29.4	74
18	3.5	89.5	106.5
25	3.5	128	157
50	4.2	200	278
50	3.5	225	280

Conclusions

The reduction in the power system noise is evident with thinner dielectrics, i.e with an increase in the capacitance and decrease in the inductance of the power planes, which leads to an overall reduction of the impedance of the planes. Thinner dielectrics can also reduce the EMI radiation at the edges of

the power plane structure. Model to measurement correlation for the source, load and noise waveforms were also shown. Experiments and simulations were done to highlight the improvements in noise suppression by using embedded capacitor laminates for decoupling high speed I/O's.
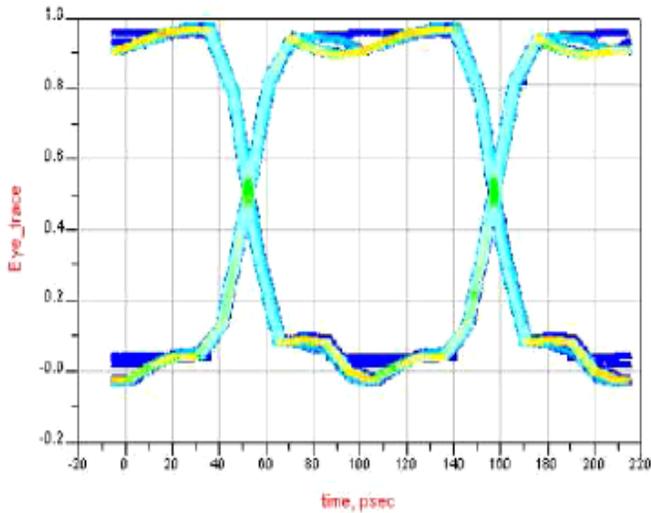

Fig. 15: Eye diagram result for the 18um thick, dielectric constant 3.5 at a differential data rate of 10Gb/s.
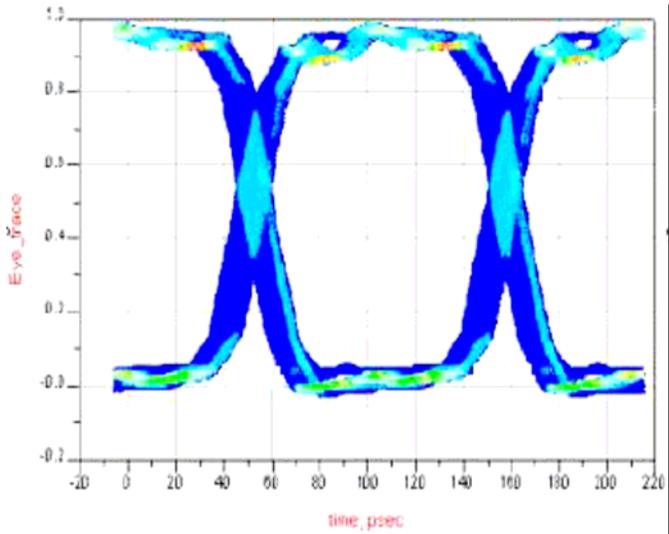

Fig. 16: Eye diagram result for the 50um thick, dielectric constant 3.5 at a differential data rate of 10Gb/s.

Acknowledgments

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