DuPont Electronic Technologies

HIGH PERFORMANCE MATERIALS

Interra™ HK 04 Series of Embedded Planar Capacitor Laminates

Design Guidelines

Introduction

DuPont™ Interra™ embedded planar capacitor laminate is used to make a set of power and ground planes within a multilayer printed wiring board. Interra™ HK 04 has 25 micron (1 mil) separation between the planes, making it ideal for low impedance at high frequency, power bus decoupling, electromagnetic interference reduction, and by-pass capacitance for discrete components.

This guide is intended to highlight design concepts associated with making the best use of DuPont™ Interra™ HK 04 embedded planar capacitor laminate. It is not intended as a comprehensive set of design rules for multilayer circuit board design and construction.

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The data in this guide is based on information generally available in the industry. However, since actual components and design strategies vary from facility to facility, the information contained herein should be used only as a guide.

For more information on DuPont's extensive range of products for Printed Wiring Board fabrication, visit our web site at http://www.dupont.com/et

PART 1: The Planar Capacitor Concept

Power and ground planes are used in multilayer printed circuit boards as a means of delivering power to discrete devices mounted on the board. Power can be either AC or DC. Power and ground planes can be made such that they comprise adjacent layers in the layer stack-up or they can be separated by one or more circuit layers. There can be more than one power plane, ground plane or pairs of power and ground planes within a board.

The intent is to deliver current and voltage when and where needed in such a way that the power supply can meet the demands of the devices without waveform degradation or large voltage fluctuations occurring at the power and ground connections of active devices. In general when a device turns on and demands current there can be a corresponding drop in voltage at the device. This is due to inherent impedance in the power distribution system caused by resistance of the copper, capacitance of the planes and the inductance associated with the spacing of the planes and circuit traces leading to the device. The classic method for supplying the needed current to the device and minimizing any voltage drop at the device is to use capacitors: large values at the point where the power supply connects to the board, medium values at certain locations on the board and small values generally placed adjacent to the power and ground pins of ICs.

The concept of a planar capacitor is to use a thin dielectric having a high capacitance between the power and ground planes. Since such planes extend across the entire substrate, through-hole vias or microvias connecting to power and ground can be placed very close to the power and ground inputs of the device, resulting in low loop inductance. DuPont™ Interra™ HK 04 has a dielectric thickness of 25 microns (1 mil) and a dielectric constant of 3.5. The thin spacing of the planes gives a capacitance density of 0.8 nF/in^2 (122 pF/cm^2). Since the planes are closely spaced, they have low inherent inductance and can therefore supply current to the device on a very short time scale, thus greatly damping fluctuations of the voltage at the device input.

A planar capacitor set of power and ground planes like DuPont™ Interra™ HK 04 could conceivably be used to reduce power bus noise in any multilayer printed circuit, but the most benefit is obtained when rise times of signals within the board are on the order of 2 nanoseconds or less. In this case, the capacitance available from the Interra™ HK 04 planar capacitor material is often enough to permit elimination of the low value surface mount capacitors placed adjacent to ICs. In addition, the low inductance associated with the close spacing of the planes contributes to overall EMI reduction.

PART 2: High Frequency

Digital IC output is nominally a square wave. A square wave is made up of the fundamental frequency and its odd harmonics. The highest frequency of the harmonic that contains significant energy is a function of the rise time of the signal pulse and can be determined by the equation:

$F = 0.35 / T_r$

Where: F = frequency in GHz
T_r = the rise time of the signal in nanoseconds

Decoupling capacitance should provide low impedance up to this frequency, which is much higher than the signaling (clock) frequency. A capacitor will exhibit decreasing impedance as frequency rises from a low level. In this frequency range the capacitor exhibits capacitive reactance. Since a capacitor has associated resistance in the leads and inductance associated with the loop area of the current path, at some frequency the capacitor will resonate and reach a minimum impedance. Beyond this resonant frequency, the capacitor will exhibit inductive reactance that increases with increasing frequency. Minimizing this inductive

reactance will minimize impedance at frequencies above the resonant frequency. Because DuPont™ Interra™ HK 04 is only 25 microns (1 mil) thick, it will have lower inductance (smaller loop area) than a discrete capacitor when used as a by-pass capacitor for an IC device. The most benefit will be gained by using HK 04 as layers 1 and 2 or as layers 2 and 3 and using microvias to connect the devices to power and ground.

PART 3: Capacitance and Inductance of Interra™ HK 04

Capacitance
The capacitance calculation in the MKS system for a parallel plate capacitor is

C in Farads [coulomb^2 / (N m)] = $\varepsilon_r \bullet \varepsilon_0 \bullet A/t$

Where ε_r is the relative permittivity of the laminate, is dimensionless and is equivalent to the dielectric constant, Dk
ε_0 is the permittivity of a vacuum and is equal to 8.85 x 10^{-12} coulomb^2 / (N m^2)
A = the area of the plates in square meters (m^2)
t = the distance between the plates in meters (m)

In the English system the calculation is

C in Farads = $\varepsilon_r \bullet \varepsilon_0 \bullet A/t$

Where ε_r is the relative permittivity of the laminate, is dimensionless and is equivalent to the dielectric constant, Dk
ε_0 is the permittivity of a vacuum and is equal to 2.25 x 10^{-13} coul^2 / (N in^2)
A = the area of the plates in square inches (in^2)
t = the distance between the plates in inches (in)

To calculate the capacitance of Interra™ HK 04 in **nanofarads** with area in **square inches** and the thickness of the dielectric in **mils** use the following formula:

C in **nF** = 0.2247 • Dk • A/t

Where Dk is the dielectric constant (or relative permittivity, ε_r)
A is the area in square inches that the power and ground planes have in common
t is the thickness in **mils** of the dielectric between the planes.

To calculate the capacitance of Interra™ HK 04 in **nanofarads** with area in **square centimeters** and the thickness of the dielectric in **microns** use the following formula:

C in **nF** = 0.885 • Dk • A/t

Where Dk is the dielectric constant (or relative permittivity, ε_r)
A is the area in **square centimeters** that the power and ground planes have in common
t is the thickness in **microns** of the dielectric between the planes.

The thin dielectric gives HK 04 a capacitance density in the range of 0.8 nF/square inch. The total capacitance of a single set of power and ground planes will depend on the total contiguous copper area that the planes have in common.

Inductance
Inductance is a function of the circuit loop area traced by a signal. Whether using Interra™ HK 04 for power distribution or as part of the decoupling network, the thin HK 04 dielectric reduces the current loop area and the corresponding inductance.

Power and Ground Plane Impedance
The impedance, Z, of a power and ground plane pair is directly proportional to the square root of the inductance, L, divided by the capacitance, C.

$Z \alpha \sqrt{(L/C)}$

Inductance is directly proportional to the thickness of the dielectric.

$L \alpha t$

Capacitance is inversely proportional to the thickness of the dielectric.

$C \alpha 1/t$

L/C is proportional to t^2.

$t \div 1/t = t^2$

$\sqrt{(L/C)}$ is proportional to the thickness, t, of the dielectric between the planes.

$\sqrt{t^2} = t$

Therefore, all other things being equal, the impedance of a power and ground plane pair is directly proportional to the thickness of the spacing between the planes.

Connection to the Power and Ground Planes
Circuit connections to the Interra™ HK 04 power and ground planes are typically done using vias: through-hole vias, buried vias, or microvias. An example of through-hole connections is shown in **Figure 1**.

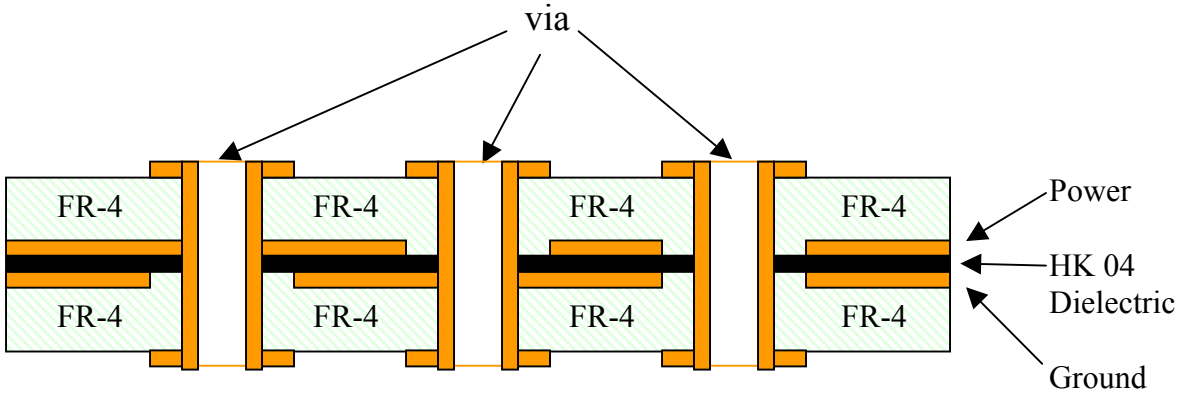


Figure 1: Typical Method of Connecting the Circuit to the Power and Ground Planes

The via on the left is connected to the top HK 04 plane. The middle via is connected to the bottom HK 04 plane. The layer between the planes is the HK 04 dielectric. The via on the right is not connected to either

plane. To provide low inductance capacitance to an IC, the IC should be mounted so that the power and ground IC pins would be attached very closely to the left and middle vias.

Figure 1 may be a little misleading. Since it is a cross sectional view, it appears that the "capacitor" is only between the left and middle vias. This is not the case with the normal use of HK 04. The "capacitor" is the entire common area of the power and ground planes.

Imaging Discrete Capacitor Areas on the Interra™ HK 04 Laminate

In some cases it may be desirable to image discrete capacitor areas on the Interra™ HK 04 power and ground planes that in cross section look something like the diagram in **Figure 2, Section A-A**.

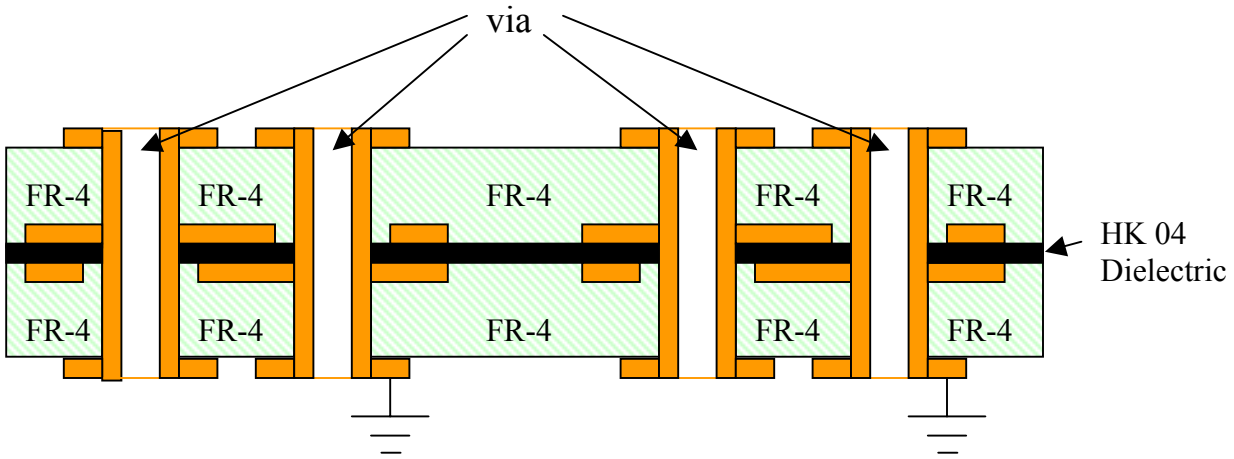


Figure 2, Section A-A

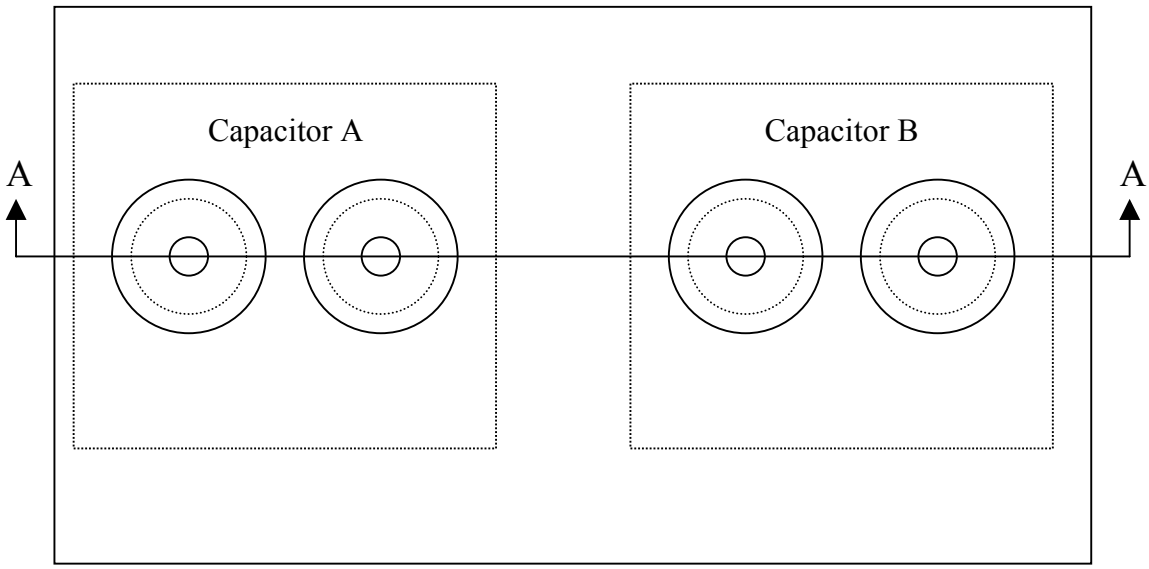


Figure 3, Plan View

In many cases the two capacitors shown, Capacitor A and Capacitor B, will have a common ground connection as depicted by the two ground symbols in **Figure 2**. The measured capacitance of Capacitor B will not be equal to the normal capacitance calculation, C (nF) = 0.2247 x Dk x A/t, where Dk is the dielectric constant of Interra™ HK 04, A is the common area of the imaged squares shown as hidden lines in

Figure 3, and t is the thickness of the HK 04 dielectric in mils. The reason is that, depending on the spacing between the two capacitors, there will be some capacitive coupling from the plates of Capacitor B to both plates of Capacitor A, which can be modeled as a parallel/series capacitor network. Measurements made on a test board of the desired construction are recommended to confirm anticipated circuit performance when imaging discrete capacitors on the HK 04 laminate.

PART 4: Power Bus Decoupling

Delivering power where needed without disruption to digital circuit performance becomes more difficult as the frequency increases. When a device requires current, the power distribution system attempts to supply the current subject to any impedance in the system. At high frequencies the DC power supply alone will not be able to deliver the required current to the device on the board and maintain the voltage needed by the device within specific limits. Discrete capacitors mounted near devices and larger capacitors mounted near the point of entry of the DC power to the board have been used to supply needed current until the current demand can be met by the supply. Failure to meet this current demand results in a voltage drop at the device and can result in signal degradation that translates into system noise. Using Interra™ HK 04 for power and ground planes provides two main benefits for the power distribution system. It acts as a large capacitor capable of discharging and providing short term current demand where needed. It also has low inductance that further reduces the impedance to current flow from the supply, permitting rapid recharging of the planes.

PART 5: EMI and Crosstalk

Any change of state of a digital or analog device will be accompanied by a voltage and current change traveling in some portion of the circuit. The traveling voltage and current can be a source of both EMI and crosstalk. There are many causes of excessive EMI. While not all of them will be addressed here, those related to the use of Interra™ HK 04 will be discussed.

Power and ground plane size, shape, and location
Grouping components will aid in EMI control because the power and ground planes will be correctly sized and placed. Examples of grouping components are:

- High voltage versus low voltage (group devices by voltage required)
- Analog devices versus digital devices
- High frequency versus low frequency
- One logic family versus another logic family

Place the power and ground planes for each group under that group so that the planes are the same shape and in register. In boards having high frequencies fringing caused by RF currents on the edges of the planes will be present. To control this fringing reduce the size of the power plane by 20 mils (0.5mm) or more (20 times the thickness of the plane's dielectric) on all outer edges.

Grouping of power and ground planes will create gaps between planes. Take care not to route signal lines that are on layers adjacent to power or ground planes across gaps in the planes. At high frequencies the current return path for a signal will follow the path of least impedance which will be on the plane adjacent to the trace and following the exact path of the trace. If the trace crosses a gap in an adjacent plane, the current return path will be forced to deviate around the gap in the plane, increasing the circuit loop area (increasing inductance) and simultaneously increasing EMI and the potential for crosstalk.

Do not route circuit lines from one group over a plane associated with a different group. Noise from currents in the different plane could capacitively couple with the signal in the trace, contributing to crosstalk. To route signal traces from one group to another, route them across the common ground.

In addition to gaps on power or ground planes caused by grouping components be aware that gaps may be purposely designed in for one reason or another. Gaps may also occur if a number of via holes are drilled in a row in close proximity in such a way as to create a gap caused by clearance holes in the power or ground plane overlapping. If a trace designed to carry a high frequency signal is routed between a set of via holes in the row, the current return path will be forced to go around the row of holes just as it would if there were a gap between planes. The general recommendation is to review the current return path that will occur on an adjacent plane directly under the trace to make sure that there are no gaps in the current return path.

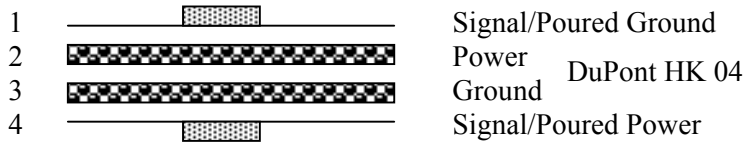
PART 6: Image Layout

Interra™ HK 04 is very flexible and strong. Therefore there are no restrictions on the amount or size of the opens that can be etched in the copper and copper can be removed from both sides of the panel in the same location.

PART 7: Layup

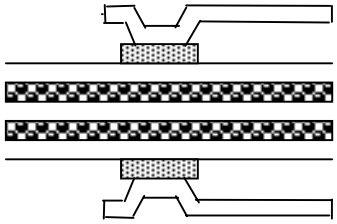
Planning for printed wiring board layer stack-up when using DuPont™ Interra™ HK 04 is important. The basic recommendation is to balance the use of HK 04 within the layup scheme. This balance concept is demonstrated by the following possible layup examples. Those that follow are not all encompassing but are considered better for high speed designs to minimize EMI and cross talk. Consultation with the engineering staff of the specific printed circuit board manufacturer is strongly recommended, at least when beginning to use DuPont HK 04, to ensure that the specified layer stack-up will not present a problem during manufacture.

Four layer board example



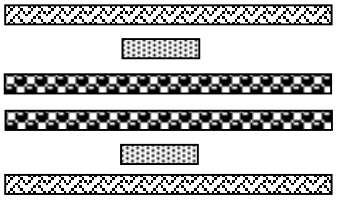
Six layer board examples

A.



1	Short Signal/Pwr	
2	Signal/Ground	HDI Layer
3	Power	
4	Ground	DuPont HK 04
5	Signal/Power	
6	Short Signal/Gnd	HDI Layer

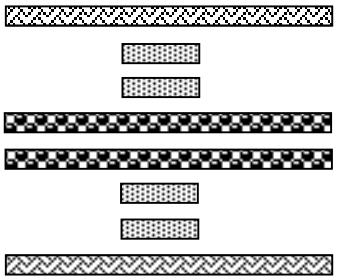
B.



1	Power	
2	Signal/Ground	
3	Power	
4	Ground	DuPont HK 04
5	Signal/Power	
6	Ground	

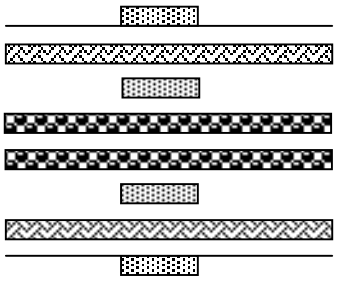
Eight layer board examples

A.



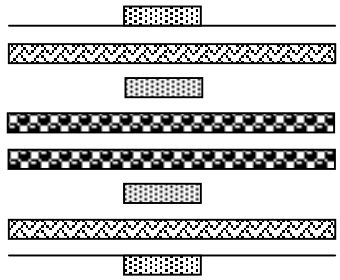
1	Ground	
2	Signal	
3	Signal	
4	Power	DuPont HK 04
5	Ground	
6	Signal	
7	Signal	
8	Ground	

B.



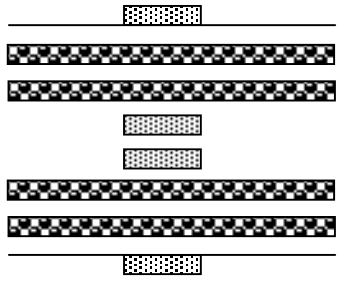
1	Signal	
2	Ground	
3	Signal	
4	Power	DuPont HK 4
5	Ground	
6	Signal	
7	Ground or Power	
8	Signal	

C.



1	Signal/Power	
2	Ground	
3	Signal/Power	
4	Ground	DuPont HK 04
5	Power	
6	Signal/Ground	
7	Power	
8	Signal/Ground	

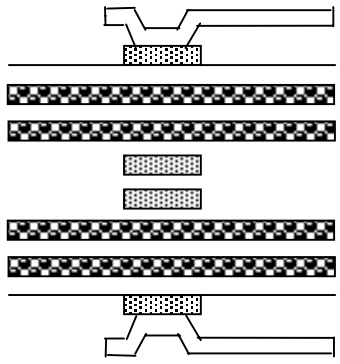
D.



1	Signal/Ground	
2	Power	DuPont HK 04
3	Ground	
4	Signal/Power	
5	Signal/Ground	
6	Power	DuPont HK 04
7	Ground	
8	Signal/Power	

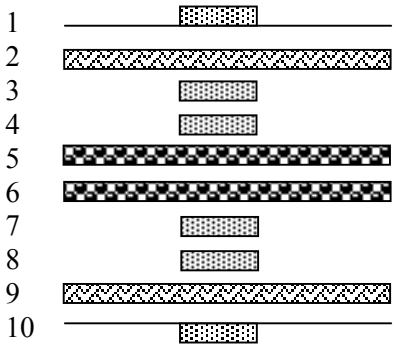
Ten layer board examples

A.



1	Short Signal	HDI Layer
2	Signal/Ground	
3	Power	DuPont HK 04
4	Ground	
5	Signal	
6	Signal	
7	Ground	DuPont HK 04
8	Power	
9	Signal/Ground	HDI Layer
10	Short Signal	

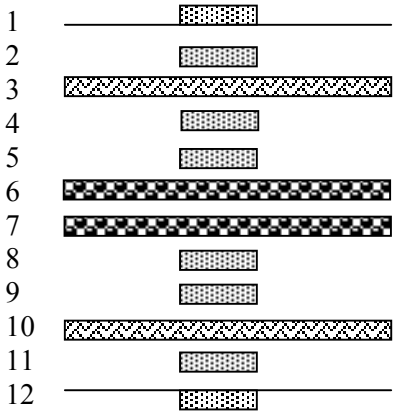
B.



1	Signal/Power	
2	Ground	
3	Signal	
4	Signal	
5	Power	DuPont HK 04
6	Ground	
7	Signal	
8	Signal	
9	Ground	
10	Signal/Power	

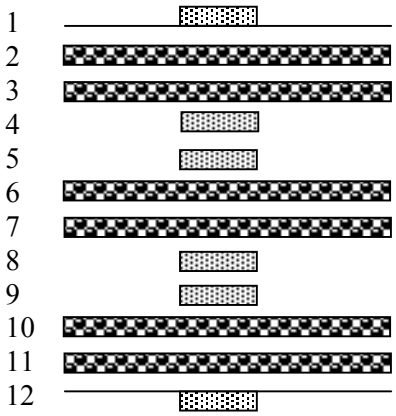
Twelve layer board examples

A.



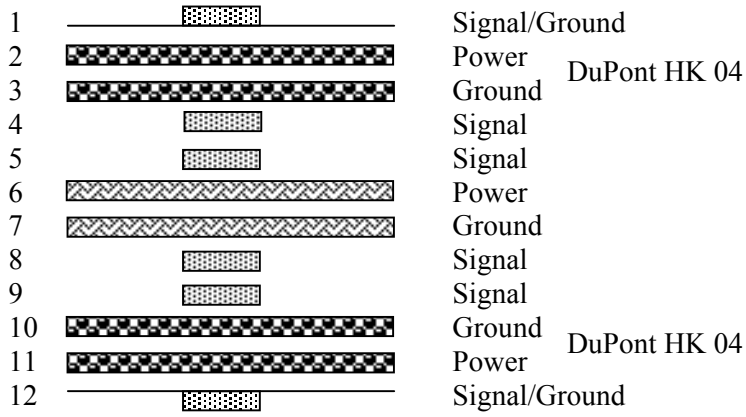
1	Short Signal	
2	Signal/Power	
3	Ground	
4	Signal	
5	Signal	
6	Power	DuPont HK 04
7	Ground	
8	Signal	
9	Signal	
10	Ground	
11	Signal/Power	
12	Short Signal	

B.



1	Signal/Ground	
2	Power	DuPont HK 04
3	Ground	
4	Signal	
5	Signal	
6	Power	DuPont HK 04
7	Ground	
8	Signal	
9	Signal	
10	Ground	DuPont HK 04
11	Power	
12	Signal/Ground	

C.



PART 8: Added Benefits

DuPont HK 04 exhibits stable capacitance density at high frequency with increasing temperature as shown in **Figure 9**. This stability means the dielectric constant remains stable with increasing temperature.

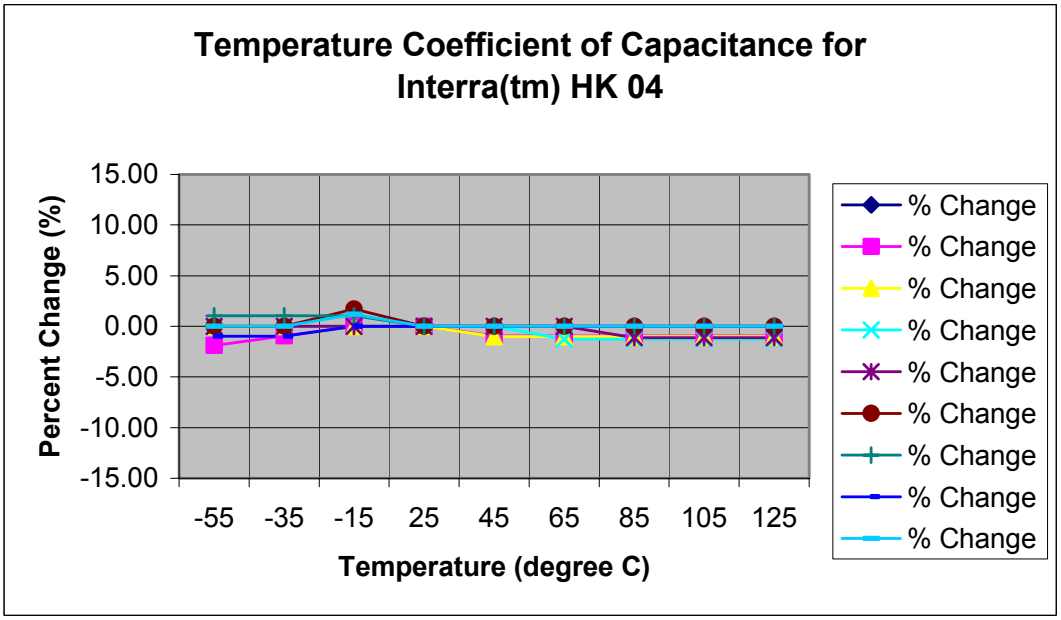


Figure 9: Capacitance density as a function of temperature of DuPont™ Interra™ HK 04

There are additional benefits that accrue when a planar capacitor material like DuPont™ Interra™ HK 04 is used. Power plane impedance reduction permits operation at lower voltage. Noise budget is improved. Surface mount capacitors can be removed, resulting in board surface area that can accommodate more silicon or can result in smaller overall board size. Board reliability is improved by elimination of SMT solder joint connections. And finally, board thickness and weight are reduced.