Next Generation Electrolytic Copper Plating Process for HDI Applications

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INTRODUCTION

Copper electroplating is a critical step in the fabrication of reliable High Density Interconnect (HDI) substrates intended for use as core layers in build–up applications. HDI substrates may contain vias and through holes having several different dimensions that make it challenging to meet via filling and hole throwing power (TP) requirements. A next generation Electrolytic Copper plating process was developed to fill blind micro vias and provide good TP in through holes to meet the demands of this market. Void-free bottom-up fill in via features with higher throwing power in through holes is achieved with this novel Direct Current (DC) copper electroplating product. The copper via fill plating bath is formulated with novel additives to operate over a wide range of operating conditions.

Consumers demand electronic products with greater capability in lighter and smaller form factors. Blind vias, buried vias and small through holes makes this possible by enabling higher circuit density. The HDI substrates used throughout this testing were 1 mm thick with 0.15 mm and 0.25 mm wide through holes. The vias were 60 µm and 100 µm deep with diameters varying from 75 to 150 µm.

This article describes the factors affecting copper electroplating for micro via filling across several via dimensions. This plating product was developed as a one-step process for use on electroless copper (0.5 - 1.5 µm) plated substrates. The new electroplating product demonstrated excellent via filling and through hole throwing power at low plated surface copper thickness.

INORGANIC COMPONENTS

The inorganic components of the copper plating electrolyte typically include copper sulfate (source of cupric ions), sulfuric acid (solution conductivity) and chloride ion. The sulfuric acid concentration range was 60-120 g/L and copper sulfate concentration range was 180-240 g/L. The chloride concentrations used were typically at ppm levels.

ORGANIC COMPONENTS

Organic additives added to plating baths are classified as carriers, brighteners and levelers. Superfilling of the vias was achieved using a combination of these additives, enabling different plating rates at the surface and inside the vias. The carriers were large molecular weight polymers. The brighteners are smaller molecular weight sulfur containing molecules. Novel proprietary levelers were used. These additives also refine the copper deposit properties.

VIA FILL GROWTH

The vias on the HDI substrates are filled by superfilling with copper. Superfilling is achieved when plating is accelerated at the bottom of vias but suppressed at the knee and at the surface. A DC copper electroplating process was developed to completely fill micro vias with copper and provide higher throwing power in through holes for HDI substrates. The filled vias were free of voids with a dimple of less than 10 microns.

Additives play a very important role in via filling processes. Therefore, selection of types and concentrations of novel additives is critical. The synergistic behavior between the additives aids in achieving void free fill. Carrier molecules, also known as suppressors, are typically larger molecular weight polymers that adsorb onto the copper surface, reducing copper deposition. Brighteners, which act as plating accelerators, are typically sulfur containing small molecules. They diffuse into the vias and accelerate copper deposition at the bottom of the vias. Levelers are adsorbed in high current density regions such as the via entrance, preventing void and bump formation.

Bottom-up fill in the via is achieved by this differential adsorption of additives at the via surface and inside the holes. During the initial stages of the plating cycle, conformal plating is observed. The carrier and leveler are adsorbed at high agitation regions such as the panel surface, suppressing the plating, while the brightener diffuses into the via bottom thereby accelerating the plating at the bottom of the via. This leads to bottom-up fill with superfilling taking place during the later stages of plating leading to complete filling of the vias without voids[1-7].

The concentration of copper sulfate and sulfuric acid is important with HDI boards since they contain both microvias and through holes. Higher copper concentration promotes via fill while higher acid promotes higher throwing power. Via filling baths that must also plate through holes must be formulated to achieve sufficient through hole throwing power while maintaining via filling performance. Copper sulfate concentrations greater than 200 g/L and sulfuric acid concentrations greater than 100 g/L were used to achieve good via fill and higher throwing power in through holes.

Plating was carried out in an R&D scale-up pilot line designed to simulate vertical in-line production. This process was developed to work with solution jet impingement and insoluble anodes in vertical batch mode, vertical in-line and horizontal conveyorized plating equipment. Eductors or nozzles were also used to further enhance fluid flow into the features.

The product was developed to fill vias of several dimension with a single chemistry that can cover a wide range of products and can be used in both panel and pattern plate mode.

VIA FILL METRICS

The schematic shown in Figure 1 illustrates how filling performance is evaluated including %Via Fill, dimple depth or bump height.

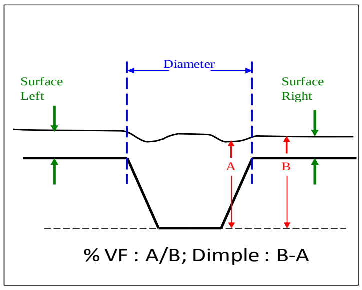


FIGURE 1. Dimple and void measurements

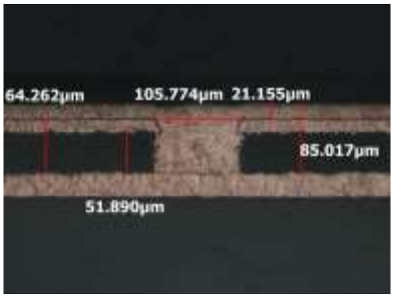


FIGURE 2. Dimple and void measurements for a 60 µm x Ø 100 µm via

A via cross-section with the corresponding measurements is shown in Figure 2. Dimple depth is the most commonly used metric. Void area, typically expressed as % void (Void Area / Hole Area) may also be calculated depending on customer requirements.

EFFECT OF CLEANER ON VIA FILLING

Via filling can be affected by the electroless substrate cleanliness and as such the substrate should be free from surface oxidation or any contamination.

Acid Cleaner	
60 µm x ∅100µm	100 µm x ∅100µm
	

Alkaline Cleaner	
60 µm x ∅100µm	100 µm x ∅100µm
	

TABLE 1. Plating performance as a function of cleaner type

Electroless substrates are processed through a preclean process prior to plating. The preclean steps include an acid or alkaline cleaner, water rinse and acid dip followed by transferring the substrate into the plating bath. The preclean steps help remove any surface oxidation or contamination and improve via fill performance. Good via fill plating is demonstrated with an Acid or Alkaline cleaner (Table 1).

EFFECT OF CURRENT DENSITY ON VIA FILLING

Solution flow rate and current density are two important factors that need to be optimized to achieve good via fill with low dimple depth and no voids. Plating studies were performed to evaluate the via filling impact of solution flow at different flow rates (low, medium and high). Good via fill and higher throwing power in through holes was achieved at medium flow rate. As a result, all data reported in this paper were collected at medium flow rate.

The effect of current density was studied at 1.5, 2.0 and 2.5 ASD. The resulting via filling performance as a function of current density is shown in Table 2. The process demonstrates consistent filling of micro-vias across a wide range of current densities. Plating was carried out at a target surface copper thickness of 21 µm. Dimple depth of less than 10 µm was achieved in the current density ranges tested.

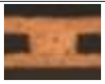
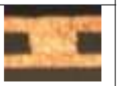
	1.5 ASD	2.0 ASD	2.5 ASD
60 µm x ∅100µm			
60 µm x ∅125µm			
100 µm x ∅ 100µm			
100 µm x ∅ 125µm			

TABLE 2. Plating performance as a function of current density

BATH PERFORMANCE WITH AGE

Excellent via filling performance and high throwing power in through holes must be achieved at low surface copper thickness with a mirror bright surface, free of nodules and flares. Plating was carried out in an R&D scale-up pilot line designed to simulate vertical in-line production up to 200 Ah/L to evaluate the via filling and throwing power performance.

This plating product was formulated for electroless copper plated substrates but can also be used for flash coupons. Pretreatment of electroless copper surfaces was required to achieve consistent via filling. The test panels were processed in a vertical batch pilot scale plating cell at bath ages from 0 to 200 Ah/L. Consistent dimple depth of less than 10 µm was maintained for 100 µm x Ø 125 µm vias. Table 3 demonstrates the process capability to fill 60 and 100 µm deep microvias at 0, 50, 100 and 200 Ah/L. All test panels were plated at a current density of 2.0 ASD.

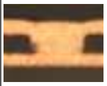
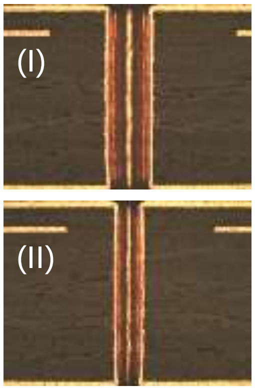
	60 µm		100 µm	
	∅ 100 µm	∅ 125 µm	∅ 100 µm	∅ 125 µm
0 Ah/L				
50 Ah/L				
100 Ah/L				
200 Ah/L				

TABLE 3. BMV performance up to 200 Ah/L at
21 µm surface copper thickness

The cross section results demonstrated that the plating bath is stable at 200 Ah/L. The product was able to meet the requirements of via fill when the bath was aged up to 200 Ah/L. The process developed may be used in either panel or pattern plate processes depending on customer requirements.

THROWING POWER

Through hole throwing power (TP) is affected by several factors such as solution conductivity, solution flow and hole geometry. These must be optimized for void free via fill with high throwing power.



I. 0.25 mm Through Hole

II. 0.15 mm Through Hole

FIGURE 3. Through hole throwing power >85% was achieved for (I) 0.25 mm and (II) 0.15 mm diameter through holes.

The throwing power data for the plating product developed is shown in Figure 3. The hole throwing power for 0.15 mm and 0.25 mm diameter through holes were greater than 85%.

SURFACE APPEARANCE AND ROLLER MARK

The coupons plated following bath ageing appeared mirror bright with very few roller marks on the surface as seen in Figure 4.

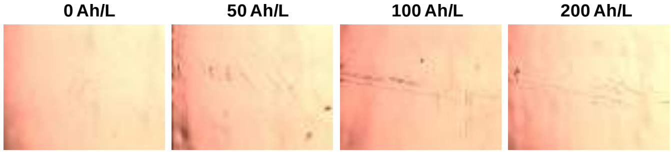


FIGURE 4. Surface and Roller mark appearance of plated coupon

RELIABILITY AND PHYSICAL PROPERTIES

Table 4 below shows the reliability test results of the plated test coupon with through holes and blind microvias. The interconnect reliability tests were performed per the procedure listed in the IPC manual[8]. The evaluation was performed by cross-section analysis after solder floating 6 times at 288°C. No cracks or other defects were detected in the copper deposit.

Current Density (ASD)	Panel TH∅ (mm)	Cross Section	Pass
2.0	0.15		✓
2.0	0.25		✓

TABLE 4. Through hole interconnect reliability

TENSILE STRENGTH AND ELONGATION

Physical properties such as Tensile Strength and Elongation were measured throughout the bath ageing at 0, 50, 100 and 200 Ah/L for this next generation Electrolytic Copper product.

Elongation of 20-30% and tensile strengths above 40 kpsi, were measured for the plated copper. The results are shown in Figures 5 and 6 respectively.

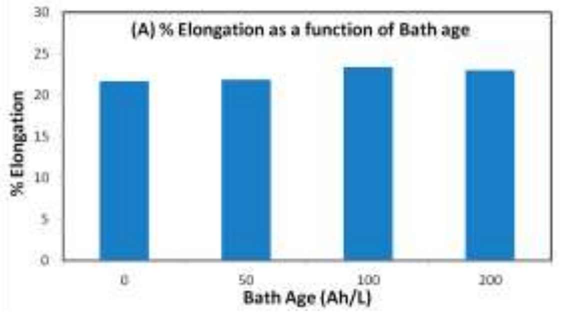


FIGURE 5. The % Elongation at 2 ASD as a function of bath age.

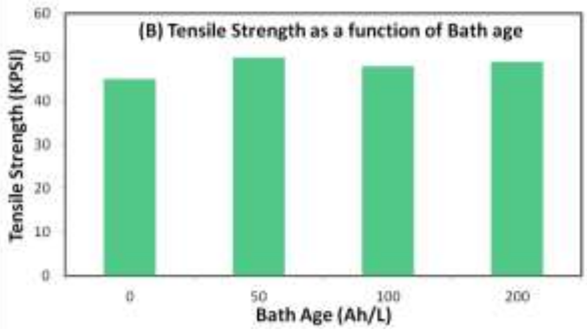


FIGURE 6. Tensile strength at 2 ASD as a function of bath age.

SUMMARY

A new DC copper electroplating product was developed that provides superior via filling performance for a wide range of via depth and via diameter. This process was developed to meet the HDI substrate demands for high volume production and can be used in both panel and pattern plate mode. This product is capable of plating a wide a range of products with a single chemistry.

The robust plating process can be operated over a wide current density range and the bath performed well when cycled up to 200 Ah/L. This new plating product can fill microvias with higher through hole throwing power while maintaining excellent physical and mechanical properties. The performance can be further improved by optimizing plating parameters utilizing either vertical or horizontal in-line plating tools depending on the customer requirements.

The novel plating product will be commercialized and will meet the current and future needs of HDI applications.

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