Millimeterwave LTCC Wafer Probe-to-Stripline Transition Using Transverse Inductive Slots

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***Abstract*— A broadband 50Ω CPW-to-stripline transition is presented which is capable of operation up to 70 GHz. This vertical transition into stripline (SL) is fabricated in DuPont 9K7 low-temperature co-fired ceramic (LTCC). It employs inductive slots in the upper SL ground plane and a circular aperture in the lower SL ground plane to tune for best return loss at 60 GHz. It is designed for wafer probing an LTCC module containing an embedded stripline. This vertically compact transition occupies only two layers of nominal 5 mil thick tape. It is also compact in the longitudinal direction, occupying less than 30 mils of longitudinal length. Both simulated and measured s parameter results are shown for back-to-back transitions up to 110 GHz. Measured insertion loss for a single transition is about 0.30 dB near 60 GHz and about 0.40 dB up to 100 GHz.**

Keywords* — *transition, low-temperature co-fired ceramic (LTCC), millimeterwave, inductive slots

I. Introduction

A necessary millimeter wave transition for LTCC module development is the CPW-to-stripline vertical transition. The reasons for this include the fact that wafer probes use CPW launchers, and stripline (SL) offers a shielded, broadband, and non-dispersive transmission line structure that is readily compatible with LTCC fabrication practices and fully utilizes the multilayer capability of LTCC.

CPW-to-stripline transitions have been published by numerous authors in recent years. Leib et. al [1] presented such a transition for microwave frequencies that was fabricated using two layers of 25 mil RT/Duroid 6010. It demonstrated good performance up to about 9 GHz. Shuo Lei et. al [2] presented a CPW-to-stripline transition design fabricated with six layers of Ferro A6M LTCC tape that was predicted to have about 2 dB of insertion loss over 50 GHz to 70 GHz band. Perrone et. al. [3] demonstrated a two tape layer transition fabricated using DuPont 951. Good return loss (~20 dB) was measured up to 67 GHz, but no insertion loss data was presented. Lee and Park [4] published a much more complex CPW-to-stripline transition that included three staggered signal vias per transition plus two multi-layer air cavities per transition. Their transition used seven LTCC tape layers. They measured an insertion loss near 60 GHz of better than 2 dB for a pair of back-to-back transitions.

The CPW-to-stripline transition presented below is believed to be one of the smallest millimeterwave LTCC transitions published to date, with a required board area of less than 30 mils by 35 mils, or less than 1 sq. mm. It also has good insertion loss, measured at about 0.30 dB up to 60 GHz for a single transition. This transition design is also vertically compact employing only two tape layers in the LTCC stackup.

II. Design Features

Fig 1 shows a cutaway view of the metal bodies that comprise the CPW-to-stripline transition. The gold conductors are the signal path. The red and green ground planes are the SL ground. All pink colored vias are grounding and shielding vias. A unique feature is the pair of inductive slots extending into the upper SL ground plane in the transverse direction. These slots add extra series inductance with minimal loss. A second feature is the circular aperture in the lower SL ground plane which is centered below the signal via [5], [6]. It's purpose is to reduce parasitic capacitance.

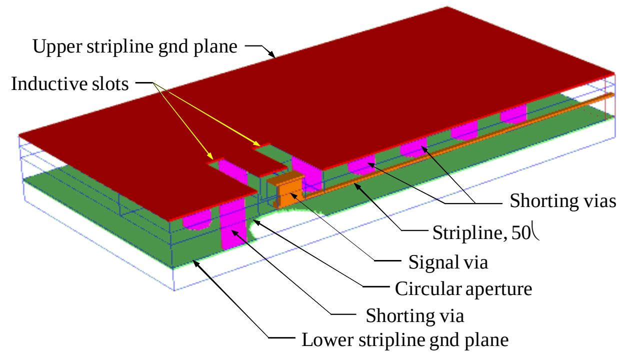


Fig. 1. Features of the proposed CPW-to-SL transition.

Fig. 2 shows a plan view with dimensions of the LTCC transition. The inductive slots in the upper ground plane along with the 6 mil sq. square signal pad forms an H-shaped pattern. Two grounding vias are located at the top and bottom of this H, and their transverse offset is defined as the variable "offset." The frequency of the predicted return loss null may be tuned by varying "offset." See section III below.

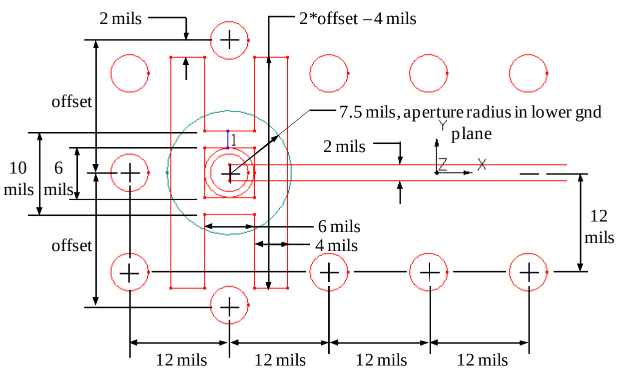


Fig. 2. Plan view of the conductors in the proposed CPW-to-stripline transition.

This transition is fabricated in DuPont Greentape™ 9K7 LTCC that is nominally 5 mils thick, with a post-fired thickness of 4.25 mils. The punched vias have a post-fired diameter of about 4.57 mils. Vias in the grounding fence have a longitudinal pitch of 12 mils, and a transverse offset of 12 mils. Au metalization is employed.

Photographs of the fabricated CPW-to-stripline transition are shown below in Fig. 3. The H-shaped slots are fabricated using laser ablation with an ultraviolet wavelength. This process forms a trench approximately 2 mils deep in the upper 9K7 tape layer the effect of which is taken into account during the design. This LTCC component was designed as a wafer probe transition to accommodate a 150 um GSG probe.

Probe tips are intended to land on the yellow crosses shown in Fig. 3(b). Also shown in this figure is a dashed yellow square which approximates a 1 mm sq. area. The entire transition fits comfortably inside this area.

III. Predicted Performance

The proposed CPW-to-stripline transition was designed using Microstripes 2012, a full wave transmission line matrix (TLM) simulation tool available from CST. A model of a single CPW-to-SL transition is shown below in Fig. 4. The corresponding solid model, shown in Fig. 1, includes a 75 mil length of 50Ω SL. A wire port is used to excite the CPW and a wave port is employed for the SL. The relative permittivity used in simulations is $\varepsilon_r = 7.0$ and $\tan\delta = .0012$ at 60 GHz. Metals are simulated with a conductivity of 3.3E7 S/m, and the planar metal bodies are 10 um in thickness. The laser ablated trenches associated with inductive slots are included in this simulation.

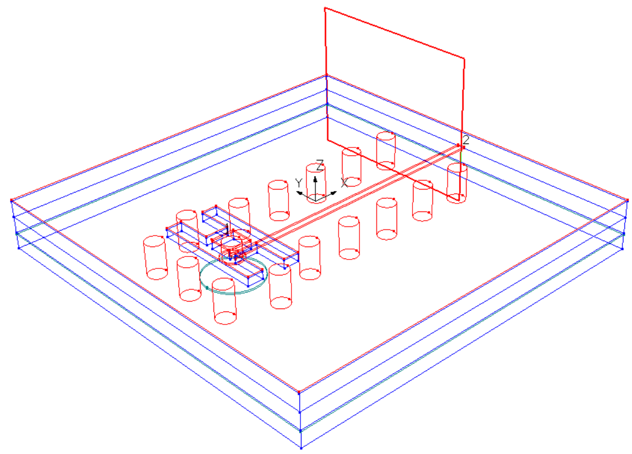
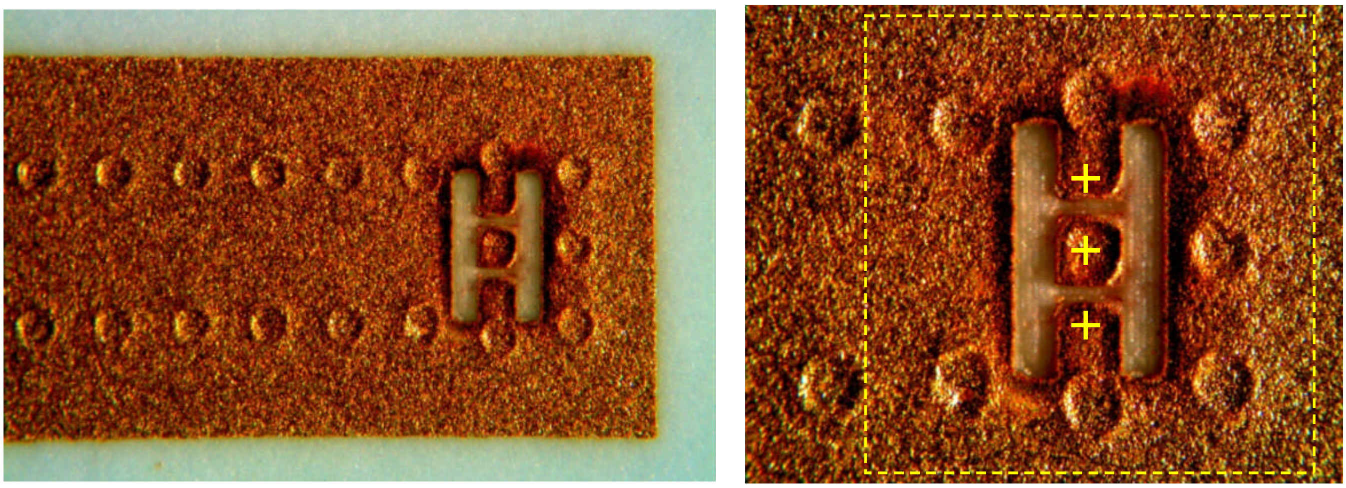


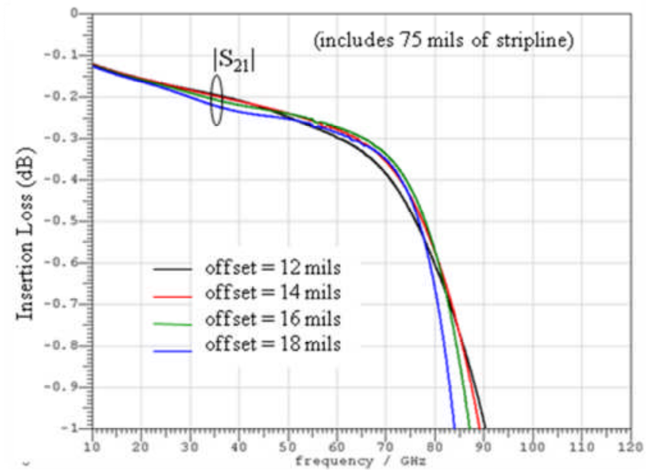
Fig. 4 Full-wave model of a single CPW-to-stripline transition.



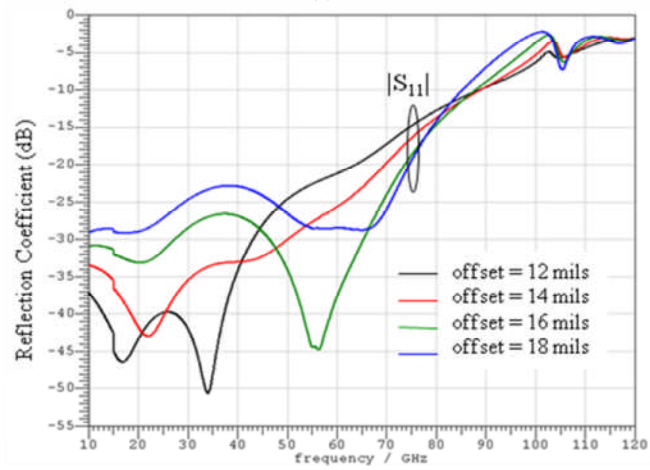
(a) (b)

Fig. 3 Photos of the proposed CPW-to-stripline transition.

Simulated performance of the single transition is shown below in Fig. 5. The parametric variable is offset, which tunes the null in reflection coefficient. There is an engineering trade between the best reflection coefficient and the broadest bandwidth. An offset of 16 mils is predicted to yield a 20 dB reflection coefficient bandwidth greater than 70 GHz. The insertion loss is a weak function of offset, as the predicted insertion loss is better than 0.30 dB (0.40 dB) up to 60 GHz (70 GHz).



(a)



(b)

Fig. 5 Predicted s parameters for the single transition of Fig. 4.

IV. Experimental Results

Back-to-back LTCC transitions were fabricated in DuPont 9K7 with SL lengths of 192 mils and 792 mils between centers of the signal vias. Fig 6 shows a 3D Microstripes model used to simulate the back-to-back transition pair with 192 mils of interconnecting SL.

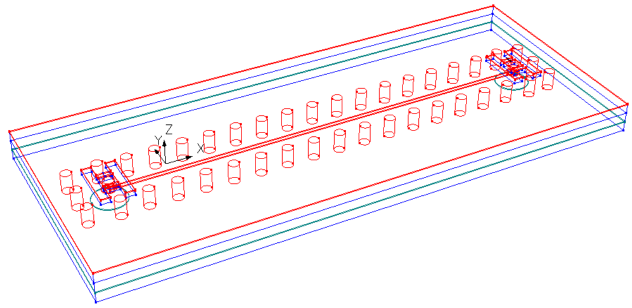


Fig. 6. Simulation model for a back-to-back transition with 192 mils of interconnecting stripline.

Measured data was recorded on transition test structures using an Anritsu model ME 7828 A Vectorstar VNA with millimeterwave test heads that allow full two port measurements up to 110 GHz. The LTCC test structures where wafer probed using a Cascade MicroTech probe station equipped with 150 um GSG probes. Two port calibration was accomplished with a planar SOLT standard.

Fig 7 below shows the simulated and measured s parameters for the back-to-back transitions shown above in Fig. 6. The predicted return loss is better than 20 dB out to 60 GHz, but the measured return loss is a little better than 10 dB up to 75 GHz.

Fig. 8 shows a detailed view of the predicted and measured insertion loss for the two back-to-back transitions of Fig. 6. The two cascaded transitions including 192 mils of 50Ω SL have a predicted (measured) insertion loss of 0.63 dB (1.45 dB) at 60 GHz. The SL insertion loss is estimated to be .848 dB at 60 GHz and .672 dB at 100 GHz using measured data from back-to-back test structures of dissimilar length. Therefore, one can estimate that the single transition measured insertion loss is about 0.30 dB at 60 GHz and 0.39 dB at 100 GHz assuming a zero length SL.

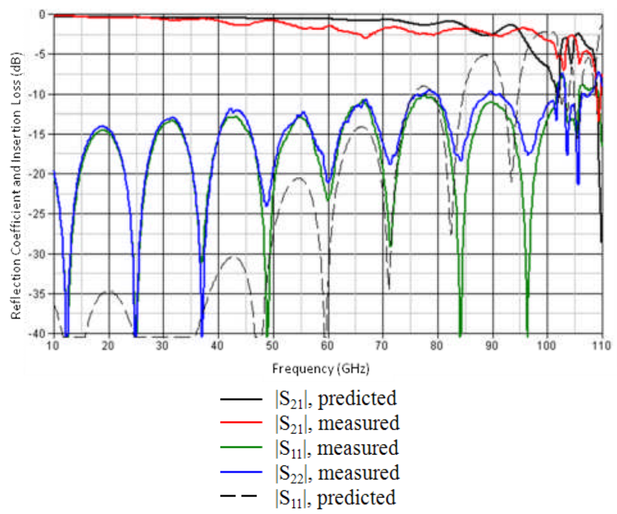


Fig. 7 Predicted and measured s parameters for the two back-to-back CPW-to-stripline transitions shown in Fig. 6 where offset = 13 mils.

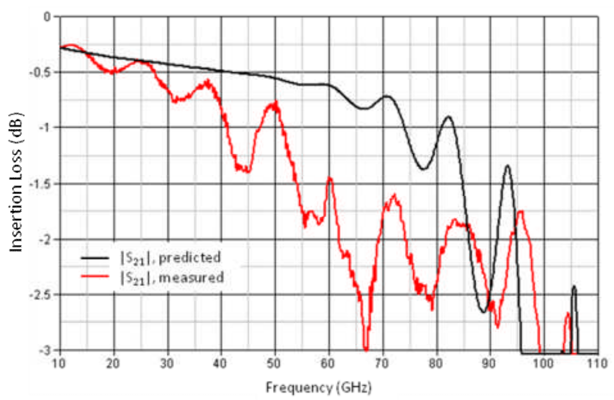


Fig. 8 Detail of the insertion loss shown in Fig. 7 for the two back-to-back CPW-to-stripline transitions illustrated in Fig. 6 where the offset is 13 mils.

V. CONCLUSIONS

This paper presents a broadband, LTCC, CPW-to-stripline vertical transition that was designed as a wafer probe interconnect for 150 um GSG probes. A single transition has about 0.30 dB of insertion loss at 60 GHz as inferred from measurements of back-to-back transitions. This transition employs a pair of transverse slots in the upper stripline ground plane to increase series inductance, and it features a circular aperture in the lower stripline ground plane to decrease parasitic capacitance. The interior stripline is completely shielded by a via fence. This compact transition easily fits inside a footprint of one square millimeter making it one of the smallest wafer probe transitions fabricated in LTCC.

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